3rd Electron Devices Technology and Manufacturing (EDTM) Conference 2019

3rd Electron Devices Technology and Manufacturing Conference (EDTM 2019)

TUTORIALS & SHORT COURSES – Register Now!

http://ewh.ieee.org/conf/edtm/2019

Conference Venue: Marina Bay Sands Convention Centre, Singapore

Date: March 12, 2019 | Time: 8:30 a.m. – 6:30 p.m.

TUT.A – Logic CMOS Device Scaling Scenarios toward N2 *Naoto Horiguchi, IMEC, Belgium* 8:30 – 10:30 a.m.	SC.A – Heterointegration: CMOS + III-V for More-than-Moore *Eugene Fitzgerald, MIT, Cambridge, USA* 8:30 – 10:30 a.m.
TUT.B – Emerging Non-Volatile Memory Technology for Storage and Computing *Daniele Ielmini, Milan Poly, Italy* 11:00 a.m. – 1:00 p.m.	SC.B – Advanced in MEMS Technology in IoT Era *Rakesh Kumar, Global Foundries Singapore* 11:00 a.m. – 1:00 p.m.
TUT.C – Advanced Packaging Technology for More Moore and More-Than-Moore *Chih-Hang Tung, TSMC, Hsinchu, Taiwan* 2:00 – 4:00 p.m.	SC.C – Technologies for Built-In Hardware Security *Massimo Alioto, NUS, Singapore* 2:00 – 4:00 p.m.
TUT.D – Progress in Back-End of Line: Materials, Characterization and Reliability *Andrew Kim, IBM Albany, NY, USA* 4:30 – 6:30 p.m.	SC.D – Designing Flexible Interactive Electronic Systems for Wearable and Implantable Applications *M.M. Hussain, KAUST, Saudi Arabia* 4:30 – 6:30 p.m.

The **3rd IEEE Electron Devices Technology and Manufacturing (EDTM) Conference** is to be held at the Marina Bay Sands Convention Centre in Singapore from March 12th - 15th 2019. As a conference sponsored by the IEEE Electron Devices Society (EDS), EDTM is rapidly becoming a premier conference for the electron devices community in the Asian region and beyond. EDTM provides a unique forum for discussion of a broad range of topics including materials, processes, devices, packaging, modeling, reliability and yield.

Day 1 (March 12) of the conference features an interesting collection of tutorials and short courses given by eminent scientists and speakers from around the world on topics of technical significance and current relevance. We have **4 tutorial sessions** on topics ranging from front-end CMOS process to back-end-of-line, packaging and non-volatile memory technology. These tutorials sessions are catered towards students and young engineers in the industry and are intended to give a comprehensive overview of the domain presenting a roadmap of the evolution of the technology over the past two decades and its possible relevance to the device technology roadmap into the future.

We also have **4 short courses** lined up for you that cover the latest advancements in niche application areas of interest, which include hardware security, sensors for IoT, flexible and wearable electronics as well as heterogeneous integration of different device technologies. The short courses are aimed at educating our attendees with the latest ongoing applied research in these four areas that will pave way for the successful realization of internet of everything (IoE), Industry 4.0 and an AI-driven economy.

The details of the tutorials and short courses (running in parallel) are provided in the next page. All courses are 2-hours long and registered attendees may choose to attend any combination of tutorials and short courses that suit their interests.

- Group discounts of **1** free registration available for **5** persons attending from a company / institution.
- Group discounts of **3** free registrations available for **10** persons attending from a company / institution.
- To register now, visit this link - https://www.conftool.org/edtm2019/

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TUT.A – Logic CMOS Device Scaling Scenarios toward N2

Naoto Horiguchi, IMEC, Belgium

8:30 – 10:30 a.m.

In recent CMOS scaling, gate and metal pitch scaling is slowing down and not enough to enable expected area reduction. Instead, track height (number of metal lines/standard cell) scaling is a main driver for CMOS area scaling today and in the future. For further 2-dimensional device area scaling or functional area scaling, device stacking technologies, such as complementary FET (CFET) and 3D sequential integration are attractive options. This tutorial starts with enablers for further scaling of contacted poly pitch (CPP) and fin pitch (FP). In addition to patterning cliff, contact resistance and gate-last integration limits further CPP and FP scaling, respectively. Key technologies for CPP/FP scaling are contact resistance reduction, spacer k value reduction, gate-last integration scaling, fin width scaling and gate-all-around (GAA) architecture introduction.

In the second part of this tutorial, the discussion centers on how to enable aggressive track height scaling toward single fin standard cell architectures, which is common in N2 node. There are two concerns in aggressive track height scaling; drive current degradation per device from fin number reduction forced by track height scaling and wiring congestions from small device area. Mobility enhancement by strain boosters and high mobility channel is important to compensate drive current degradation per device. GAA, especially stacked nanosheet is an attractive device architecture not only to improve electrostatics at short gate length but also to improve drive current in single fin architectures. Wiring congestions from small track height have to be improved by so called “scaling boosters” such as self-aligned gate contact and metal gate cut. Finally, paths for device stacking and their integration challenges are discussed. CFET, which is consisted of stacked NMOS and PMOS, is an interesting option for further area scaling of logic and SRAM. 3D sequential integration enables functional area scaling by different functions, such as logic, memory, analog and I/O.

TUT.B – Emerging Non-Volatile Memory for Storage and Computing

Daniele Ielmini, Milan Poly, Italy

11:00 a.m. – 1:00 p.m.

In the era of big data, semiconductor memory devices must fulfill two main tasks: (i) storing a large amount of data in fast, high density, nonvolatile memory arrays, and (ii) facilitating computation within the data, to enable machine learning algorithms with improved speed and energy efficiency. To meet these challenging objectives, a class of emerging memory technologies are currently being developed. Device concepts include resistive switching memory (RRAM), phase change memory (PCM), spin-transfer torque magnetic memory (STT-MRAM) and ferroelectric memory (FeRAM). These devices have unique physical mechanisms, technology, and reliability issues that require detailed understanding from the materials, device, circuit, and algorithm standpoints.

In this tutorial, I will provide an overview of the physical mechanisms of switching, the device architecture, and the technology demonstrators for the main nonvolatile emerging memories. The applications as potential RAM/Flash replacement, embedded memory, and storage lass memory will be reviewed, with reference to the array architecture, e.g., crosspoint or transistor-selected structure. A brief overview of the selector technology for high density crosspoint arrays will be given. Finally, the opportunities for in-memory computing with emerging nonvolatile memories will be summarized for analogue, digital, and neuromorphic computing scenarios.

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TUT.C – Advanced Packaging Technology for More Moore & More-Than-Moore

Chih-Hang Tung, TSMC, Taiwan

2:00 – 4:00 p.m.

An old name with a new meaning, advanced packaging technology has emerged as a new way of achieving continuous microelectronics devices function/value improvement that was previously sustained by Moore's Law transistor scaling for over 50 years. This tutorial starts by delineating the background challenges with Moore's Law and the semiconductor industry as a whole, including existing packaging technology and supply chain. This is followed by showing new market driving forces calls for new packaging technologies with value proposition, and how the eco-system/supply-chain evolved with the new market drivers.

Next, a broad review on innovative packaging technology platforms proposed by academia, foundry, and OSAT is presented. Finally, the challenges that arise as the new system integration technology platforms evolve to meet the new market diversification, including IoT, Autonomous Driving, AI and Machine Learning, and also other forward-looking applications are discussed.

TUT.D – Progress in Back-End of Line: Materials, Characterization and Reliability

Andrew Kim, IBM Albany, NY, USA

4:30 – 6:30 p.m.

As BEOL reliability is an important part of semiconductor technology development and qualification, it is of critical importance to understand materials, integration schemes, and characterization of device and reliability. The BEOL wear-out mechanisms include Electromigration (EM), Stress migration (SM), Low-k time-dependent-dielectric-breakdown (TDDB), thermal cycling, Chip-Package-Interactions (CPI), and self-heating of BEOL interconnects. This tutorial will provide key progress of BEOL process/integration and introduction of BEOL reliability physics fundamentals/models. Discussions will also be made on the BEOL reliability challenges with new materials and technology scaling.

SC.A – Heterointegration: CMOS + III-V for More-than-Moore

Eugene Fitzgerald, MIT, Cambridge, USA

8:30 – 10:30 a.m.

Moore's Law, as characterized by the scaling of device dimensions, is slowing dramatically as it reaches its end, due to both fundamental physical limits as well as economic realities of producing ever smaller transistors on ever larger wafers with sufficient throughput and yield. A new paradigm is needed, and the way forward is to use different semiconductors materials to access their superior electronic and optical properties over Si CMOS. III-V compound semiconductors, with their wide range material parameters, are ideal for pairing with existing Si CMOS process technologies.

In this short course, I will go through the benefits of hetero-integration, after which I will briefly introduce the three main paths for incorporating III-V materials into traditional Si CMOS integrated circuits.

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These are: i) replacing Si device channel (active) regions with III-Vs; ii) using packaging techniques to create multi-chip solutions; and iii) interconnecting III-V and Si devices at the circuit level to form monolithically integrated Si CMOS + III-V ICs. I will show why the monolithically integrated approaches are the best option for high growth in a More than Moore future, and how market, implementation and technology factors interact to set constraints on industry-viable solutions. I will then provide an overview of the efforts being carried out in this space at the Singapore-MIT Alliance for Research and Technology's Low Energy Electronic Systems (SMART LEES) Interdisciplinary Research Group, and how our work is paving the way towards the integrated circuits of the future.

SC.B – Advanced in MEMS Technology in IoT Era
Rakesh Kumar, Global Foundries Singapore
11:00 a.m. – 1:00 p.m.

Micro Electromechanical Systems (MEMS) technology has led the development of sensors used for variety of applications in consumer, automotive, industrial, communication, security, home automation and bio-medical fields. In the last decade, MEMS sensors have seen a rapid growth, mainly in consumer and mobile applications due to their miniature sizes, low power operations and cost effectiveness. This growth is expected to continue as more and more sensors are being designed and deployed to interact with environment to enable building of smart systems in this era of Internet of Things (IoT). The course will review the recent development in MEMS technologies and emergence of novel sensors specifically for emerging applications in mobile, autonomous vehicles, wearables and bio-medical fields. The course will cover different types of MEMS sensors and actuators, their working principles and applications. Details of MEMS design, fabrication techniques, packaging and testing of MEMS devices will be discussed along with challenges associated with manufacturing and commercialization of MEMS devices.

SC.C – Technologies for Built-In Hardware Security
Massimo Alioto, NUS, Singapore
2:00 – 4:00 p.m.

Hardware security has become a crucial aspect in the design of today's Systems on Chips (SoCs), in view of their unprecedented level of pervasiveness and connectivity. Indeed, a wide range of applications and systems require security to be rooted on hardware, due to tight resource constraints or demanding levels of security (e.g., connected devices, automotive, blockchain and crypto-currency e-wallets). Hardware security is now being explicitly demanded by users, a major area of interest for the entire semiconductor industry, and a highly inter-disciplinary research domain embracing integrated circuit manufacturing and design.

In this tutorial, hardware security is introduced in an accessible manner from the ground up, from foundations to cutting-edge techniques, while gaining an insight into the requirements of real-world applications. Techniques to create on-chip security primitives for root/chain of trust are discussed, ranging from PUFs, to TRNGs, lightweight ciphers, devices/sensors for physical integrity assurance, and counteraction of advanced attacks (from non-invasive to invasive). Emphasis is given on low-cost techniques for security down to low-end devices, for pervasive adoption. At the end of the tutorial, attendees will be able to understand basic principles of hardware security, its state of the art, and the challenges ahead.

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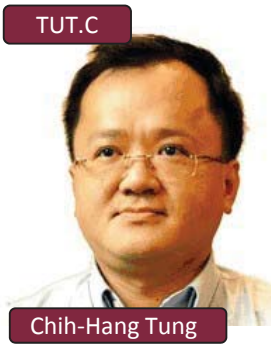
SC.D – Designing Flexible Interactive Electronic Systems for Wearable and Implantable Applications
M.M. Hussain, KAUST, Saudi Arabia
4:30 – 6:30 p.m.

For the last sixty years, miniaturization of electronics fabricated on prominent active electronic materials like silicon, germanium, III-V materials and gallium nitride has enabled modernization of today's world - specially bringing convenience, safety and efficiency in our daily life. However, we are in continuous pursuit to find out alternative materials and process technologies to lower the cost of manufacturing and to increase functionalities of electronics. A radical physical change of from rigid electronic components and systems to a mechanically compliant, flexible and stretchable version will jettison the interfacial architectural mismatch with nearly all natural lives, enhance the functionalities of existing applications and will usher into new applications, which are not possible today. In this short course, the following key areas of this emerging area of electronics will be discussed - *a. Materials, b. Design and mechanics, c. Integration strategies, d. Applications* and *e. Future Outlook*.

TUTORIAL SPEAKERS

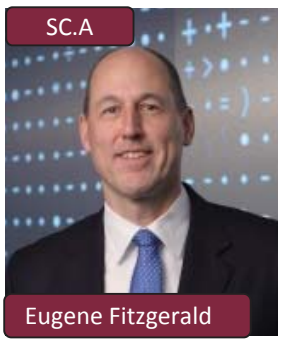

TUT.A
Naoto Horiguchi


TUT.B
Daniele Ielmini


TUT.C
Chih-Hang Tung


TUT.D
Andrew Kim

SHORT COURSE SPEAKERS


SC.A
Eugene Fitzgerald


SC.B
Rakesh Kumar


SC.C
Massimo Alioto


SC.D
M.M. Hussain