Guadalajara Section - Distinguished Lecture Series

Signal Processing & Circuits and Systems Chapter

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Universidad de Guadalajara, CUCEI,
Auditorio: Nikolai V. Mitskievich

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Memory Interfaces - Past, Present and Future.
By Dr. Timothy (Tim) Hollis

Registration Link

Abstract: DRAM standards have evolved tremendously over the last two-and-a-half decades, leading to diversification not only in the architecture of the memory array but also in that of the off-chip interface. Application-specific signaling channels have influenced the transceiver design nearly as much as system power and bandwidth requirements have. The influence of the multi-drop server channel, along with a broad range of target environments, has led the DDR branch of JEDEC DRAMs to incorporate multi-tap Decision Feedback Equalization to maximize flexibility, while shrinking supply voltages to facilitate energy reduction have led Low-Power DDR (LPDDR) to completely rethink the output driver structure. In parallel, Graphics DDR (GDDR) has reached speeds requiring nearly equal care of the external channel and the chip itself. The adoption of multi-level signaling in GDDR6x and GDDR7 to relax on-chip frequency requirements has only heightened the need for more rigorous co-design of transceiver, package and system characteristics. And, of course, the integration of silicon interposers to support High Bandwidth Memory (HBM) has driven a paradigm shift in memory interface design. With all of these adaptations, and many others not captured here, the splintering DRAM family continues to push the boundaries of single-ended signaling into the future.
This presentation briefly explores what has driven the diversification in DRAM signaling schemes over the decades, will discuss the motivation behind present embodiments, and will project into the future to where the DRAM interface is likely headed (e.g., features and functions necessary for continued energy-efficient bandwidth scaling).

Speaker Bio:

Tim Hollis received the Ph.D. degree in electrical engineering from Brigham Young University, Provo, UT, USA, in 2007.
In 2006, he joined the Advanced Architecture Group at Micron Technology in Boise, Idaho, USA where he contributed to several pathfinding activities including the first-generation Hybrid Memory Cube. From 2012 to 2014, he worked as a chipset architect at Qualcomm in San Diego, CA, USA. He returned to Micron in 2014, where he currently leads the Interface Pathfinding Group as a Micron Fellow. He has published 18 articles in journals, conference proceedings, and technical magazines, and holds 228 issued U.S. and international patents.

Dr. Hollis has been serving as a member of the IEEE Workshop on Microelectronics and Electron Devices Organizing Committee since 2010, including the General Chair in 2013. He has served on other IEEE conference committees as well as DesignCon's Technical Program Committee from 2013 to 2015. From 2017 to 2020 he served as the Technology Editor for the IEEE Solid-State Circuits Magazine and as a Guest Editor for memory- and interface-related special issues in 2016 and 2019, respectively.