TECHNISCHE UNIVERSITÄT
IN DER KULTURHAUPTSTADT EUROPAS
CHEMNITZ

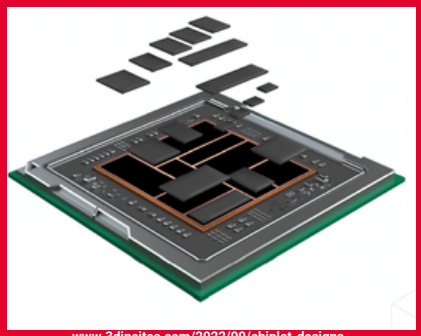
Fakultät für Elektrotechnik und Informationstechnik

Professur Werkstoffe und Zuverlässigkeit mikrotechnischer Systeme

FAKULTÄTSKOLLOQUIUM

Chiplet Design and Heterogeneous Integration Packaging

IEEE ELECTRONICS PACKAGING SOCIETY



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Chiplet is a chip design method and heterogeneous integration is a chip packaging method. Chiplet design and heterogeneous integration packaging have been generated lots of tractions lately. For the next few years, we will see more implementations of a higher level of chiplet designs and heterogeneous integration packaging, whether it is for cost, time-to-market, performance, form factor, or power consumption.

Vortragender:

Dr. John Lau

28 OKTOBER 2024

13:30 BIS 15:15 UHR

Zentrales Hörsaal- und Seminargebäude
Raum: 2/N012 (alt: C10.012)
Reichenhainer Str. 90 | 09126 Chemnitz

Zugang Online-Stream:

Alle Zuhörer sind von 13:30 bis 13:45 Uhr zum Kaffee im Foyer des Hörsaalgebäudes eingeladen.

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Informationen zum Vortrag erteilt:
Prof. Dr. Bernhard Wunderle,
IEEE EPS Germany

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Montag, 28 Oktober 2024
13:30 bis 15:15 Uhr

Ort:
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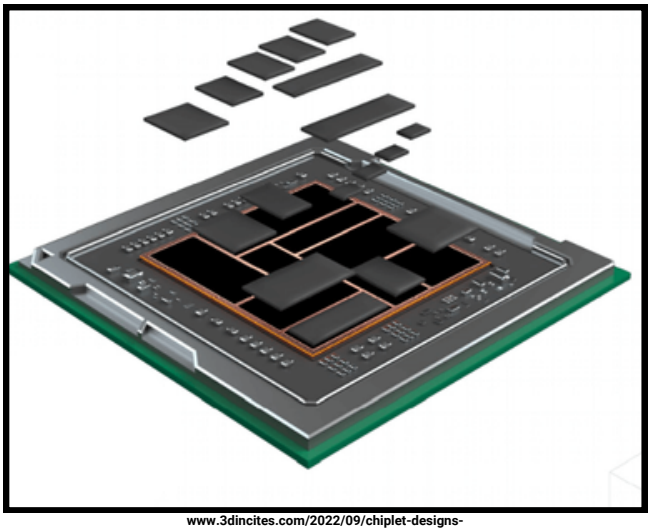
CHIPLET DESIGN AND HETEROGENEOUS INTEGRATION PACKAGING

Chiplet is a chip design method and heterogeneous integration is a chip packaging method. Chiplet design and heterogeneous integration packaging have been generated lots of tractions lately. For the next few years, we will see more implementations of a higher level of chiplet designs and heterogeneous integration packaging, whether it is for cost, time-to-market, performance, form factor, or power consumption. In this lecture, the following topics will be covered.

- System-on-Chip (SoC)
- Why Chiplet Design?
- Chiplet Design and Heterogeneous Integration Packaging – Chip Partition and Chip Split
  - Chip partition and Heterogeneous Integration
  - Chip split and Heterogeneous Integration
- Communication between Chiplets (e.g., Bridges)
  - Bridge Embedded in Build-up Package Substrate
  - Bridge Embedded in Fan-Out EMC with RDLs
  - UCIe
  - Hybrid Bonding Bridge



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- Chiplet Design and Heterogeneous Integration - Multiple System and Heterogeneous Integration
  - Multiple System and Heterogeneous Integration with Package Substrate (2D IC Integration)
  - ...with Thin Film layer on the Package Substrate (2.1D IC Integration)
  - ...with TSV-less (Organic) Interposer (2.3D IC Integration)
  - ...with Passive TSV-Interposer (2.5D IC Integration)
  - ...with Active TSV-Interposer (3D IC Integration)
- Advanced Packaging Driving by AI
- Co-Packaged optics
- Potential R&D Topics in Chiplet Design and Heterogeneous Integration Packaging
- Trends in Chiplet Design and Heterogeneous Integration Packaging

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