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Universal Chiplet Interconnect Express™ (UCIe™): An Open Interconnect Standard for Innovations On-Package

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17:00 (Israel Time), online Zoom session

Registration is free. Please register here (Zoom link will be provided after registration)

Abstract

A High-performance workloads demand on-package integration of heterogeneous processing units, on-package memory, and communication infrastructure such as co-packaged optics to meet the demands of the computing landscape. On-package interconnects are a critical component to deliver the power-efficient performance with the right feature set in this evolving landscape. Universal Chiplet Interconnect Express (UCIe) is an open industry standard with a fully specified stack that comprehends plug-and-play interoperability of chiplets; like the seamless interoperability on board with well-established and successful off-package interconnect standards such PCI Express® and Compute Express Link (CXL)®. In this talk, we will discuss the usages and key metrics associated with different technology choices in UCIe and how it will evolve going forward from a planar interconnect (2D/ 2.5D) to 3D to deliver superior power-performance metrics. We will also delve into the challenges and opportunities for chiplets connected through UCIe.

Bio

Dr. Debendra Das Sharma is an Intel Senior Fellow and co-GM of Memory and I/O Technologies, Data Platforms and Artificial Intelligence Group, at Intel Corporation. He is a leading expert on I/O subsystem and interface architecture. He delivers Intel-wide critical interconnect technologies in Peripheral Component Interconnect Express (PCIe), Compute Express Link (CXL), Universal Chiplet Interconnect Express (UCIe), and Intel's Coherency interconnect, as well as their implementation. Dr. Das Sharma is a member of the Board of Directors and treasurer for the PCI Special Interest Group (PCI-SIG). He has been a lead contributor to PCIe specifications since its inception. He is the co-inventor of CXL, a founding member of the CXL consortium, and chairs the CXL consortium. He co-led the CXL Board Technical Task Force (2019-2024) and is a leading contributor to CXL specifications. He co-invented the chiplet interconnect standard UCIe and is the chair of the UCIe consortium.Dr. Das Sharma has a bachelor's in technology (with honors) degree in Computer Science and Engineering from the Indian Institute of Technology, Kharagpur and a Ph.D. in Computer Engineering from the University of Massachusetts, Amherst. He holds 190+ US patents and 500+ patents world-wide. He is a frequent keynote/ plenary speaker, distinguished lecturer, invited speaker, invited columnist, and panelist at Nature Electronics, IEEE International Test Conference, IEEE Hot Interconnects, IEEE Cool Chips, IEEE 3DIC, SNIA SDC, PCI-SIG Developers Conference, CXL consortium, Open Server Summit, Open Fabrics Alliance, Flash Memory Summit, Intel Innovation, and Universities (CMU, Texas A&M, Georgia Tech, UIUC, UC Irvine). He has been awarded the Distinguished Alumnus Award from Indian Institute of Technology, Kharagpur in 2019, the IEEE Region 6 Outstanding Engineer Award in 2021, the first PCI-SIG Lifetime Contribution Award in 2022, the IEEE Circuits and Systems Industrial Pioneer Award in 2022, and the IEEE Computer Society Edward J. McCluskey Technical Achievement Award in 2024