Co-Packaged Optics:
Heterogeneous Integration of Photonic IC and Electronic IC
(IEEE Electronic Packaging Society - Central Indiana chapter)

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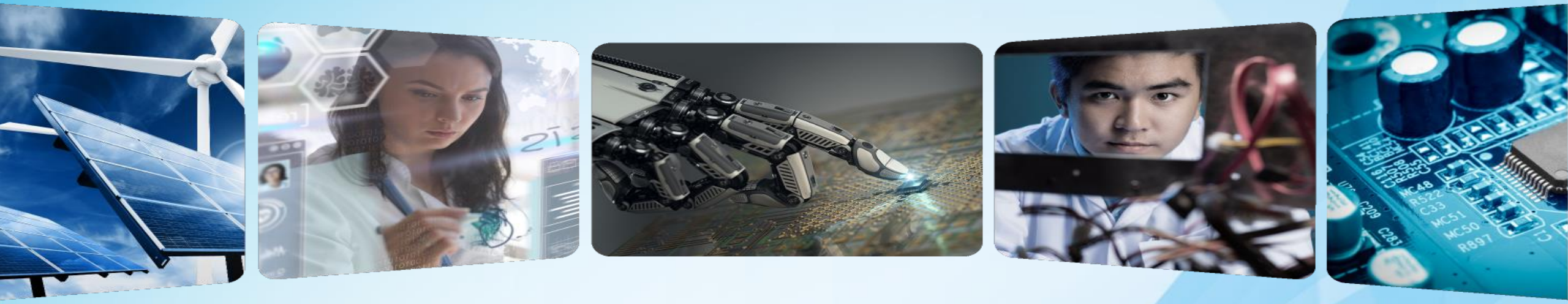
March 5, 2024



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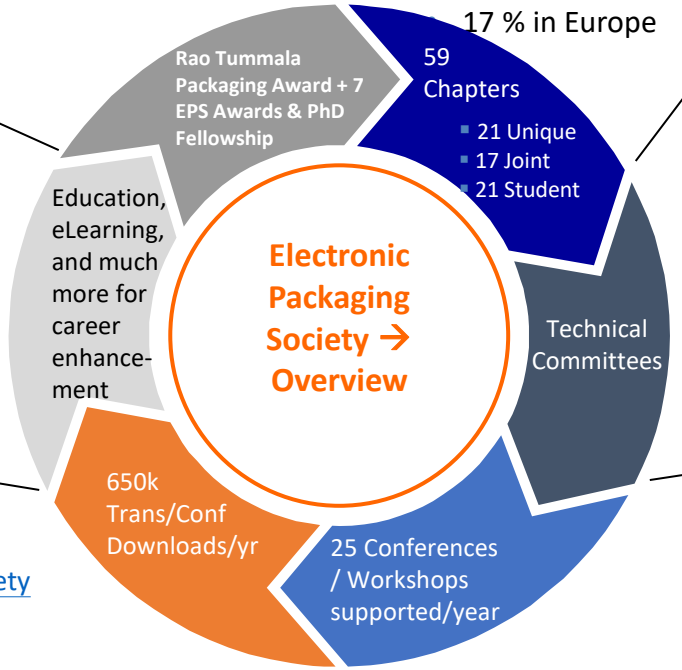

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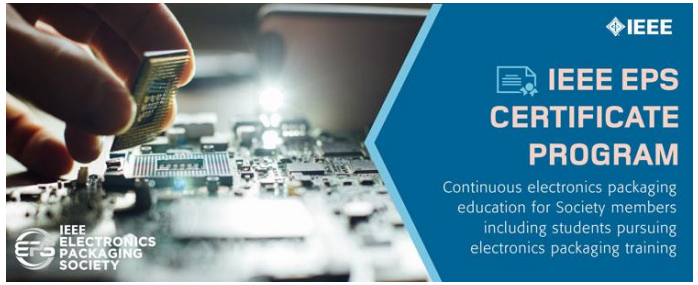

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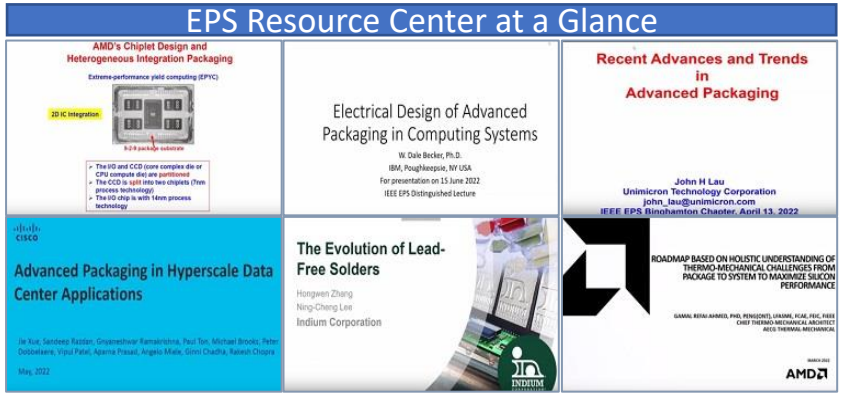

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CONTENTS

Silicon Photonics

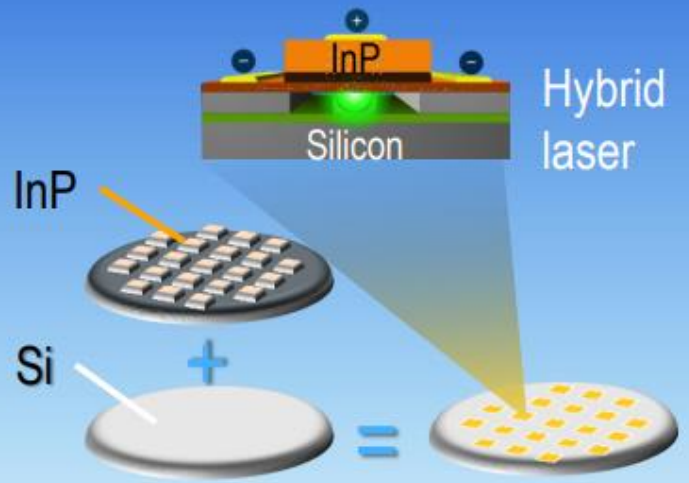
Is for

Silicon

INTEGRATION

Intel Silicon Phonics: Optics at Silicon Scale

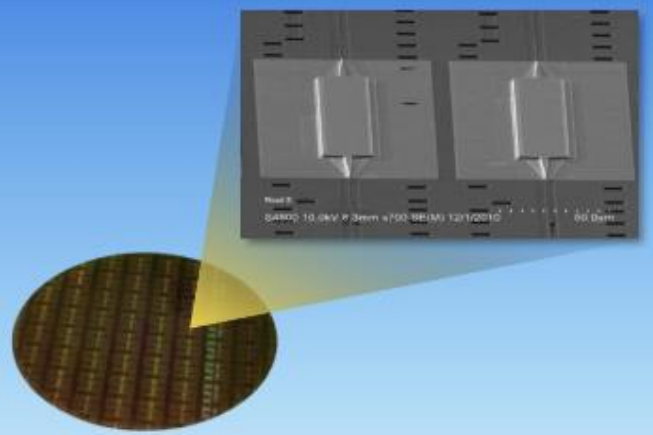
Silicon Integration



Integrated Optics, Enabled by Intel's Hybrid Laser Technology

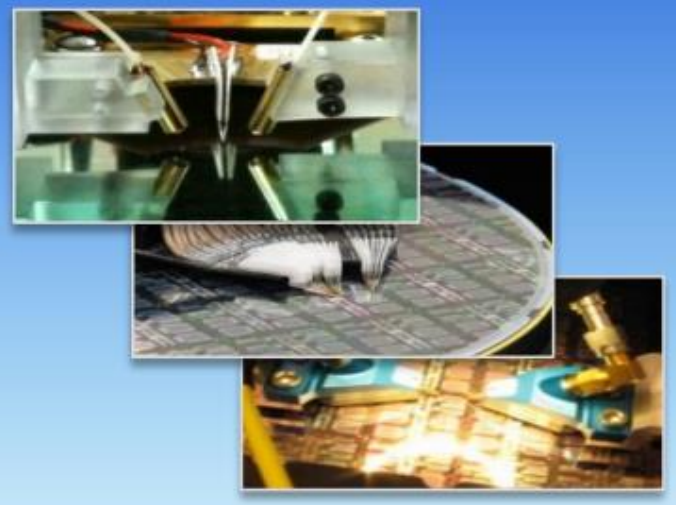
InP for lasers, SOAs, PDs

Silicon Manufacturing



Advanced CMOS Mfg Process at Intel Fabs On 300mm Wafers

Silicon Scale



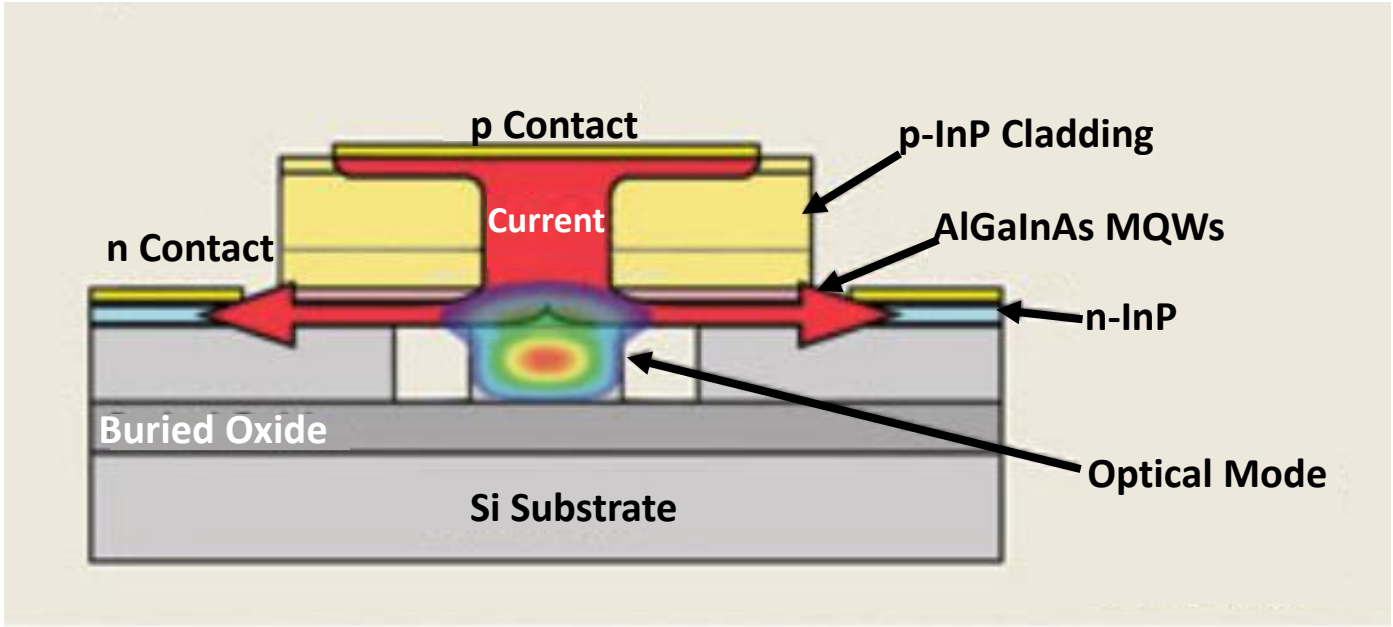
Automated On-wafer Optical, Electrical, and High-speed Test

Wafer-level burn-in

Wafer-scale manufacturing of optical sub-assembly; known good die at wafer level

A hybrid silicon laser. (a) Key components. (b) Scanning electron micrograph of the fabricated device. (c) Schematic.

(a)



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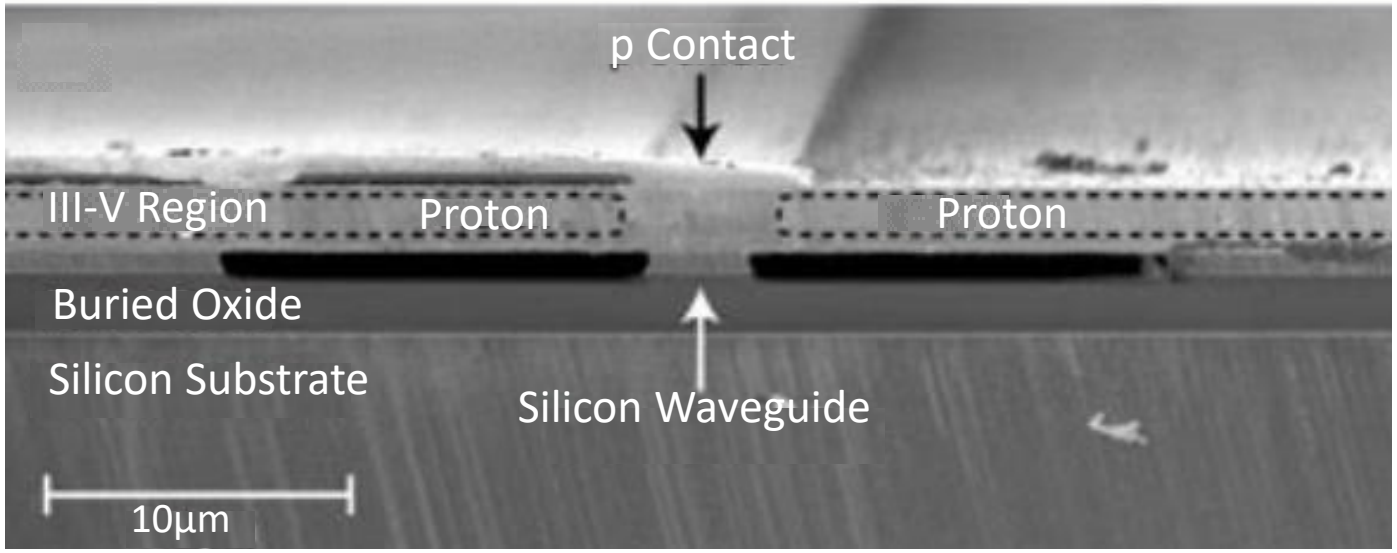

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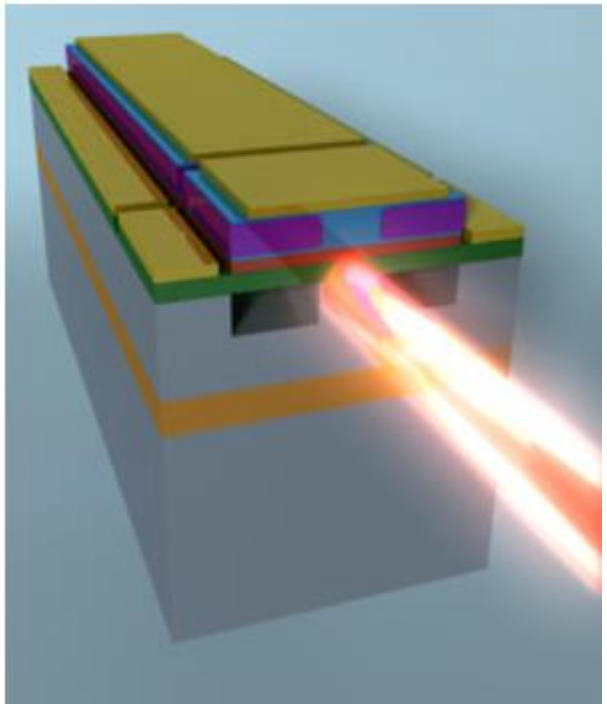


Indium phosphide (InP), the light-emitting material, is bonded to the top of the silicon with a thin layer of glass glue.

Intel is the only company who is in high volume manufacturing of Silicon Photonic

Co-Packaged Optics (CPO)

or

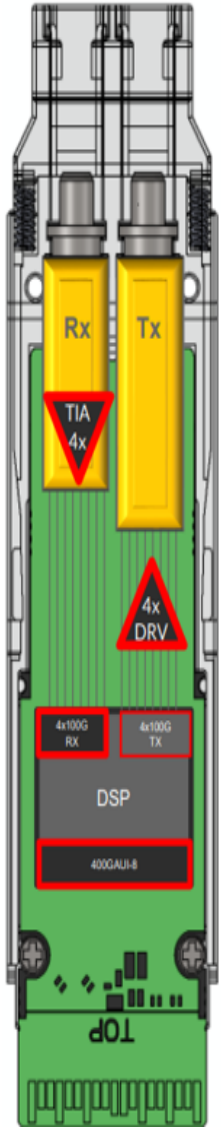
Heterogeneous Integration of Electrical IC (EIC) and Photonic IC (PIC) Packaging

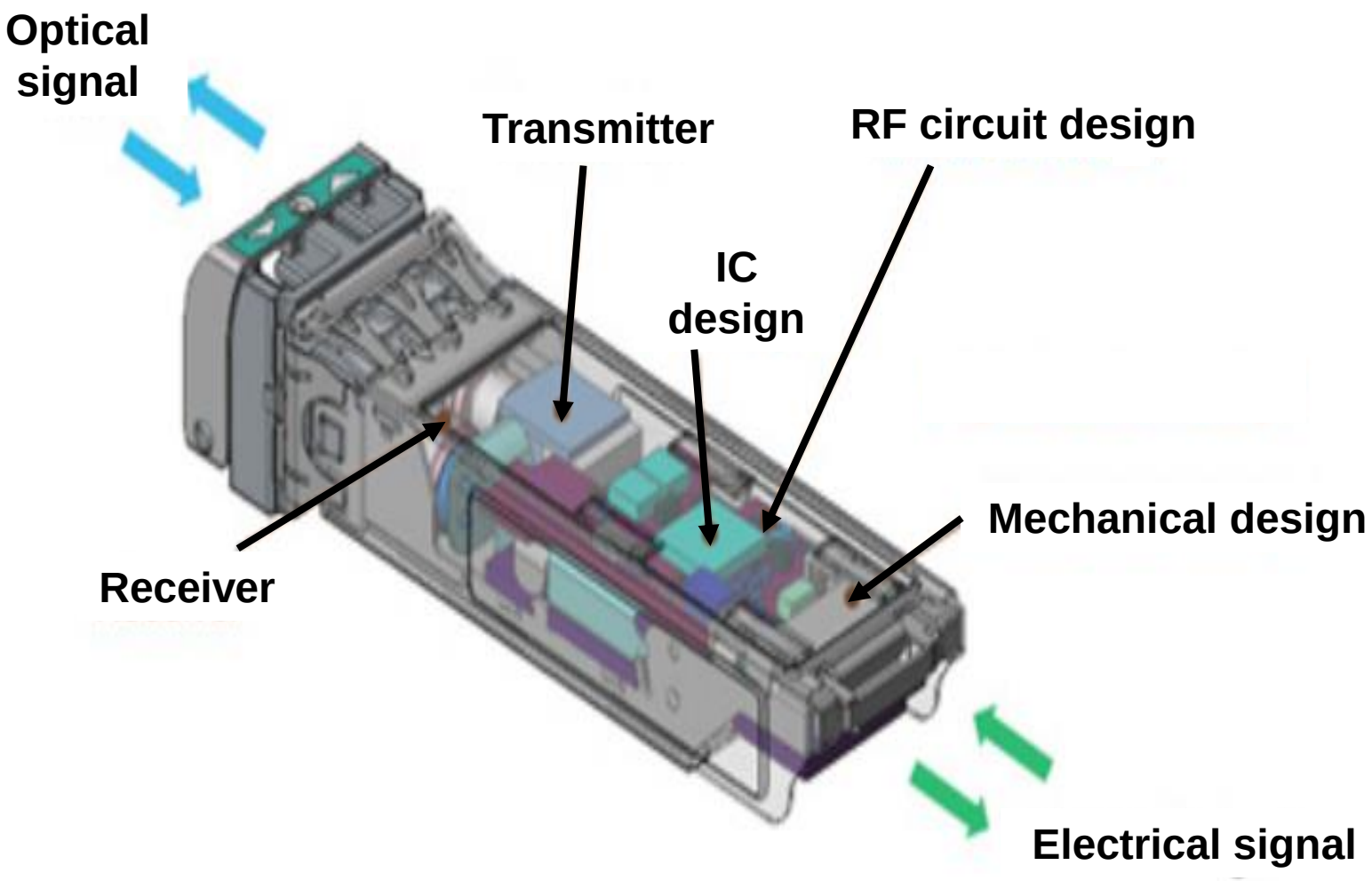
(a) Google data center. (b) Transceivers in a data center.

(a)

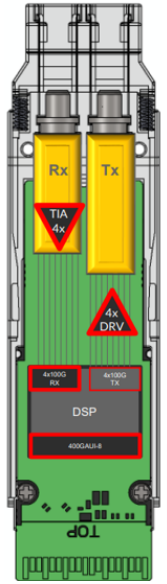
(b)

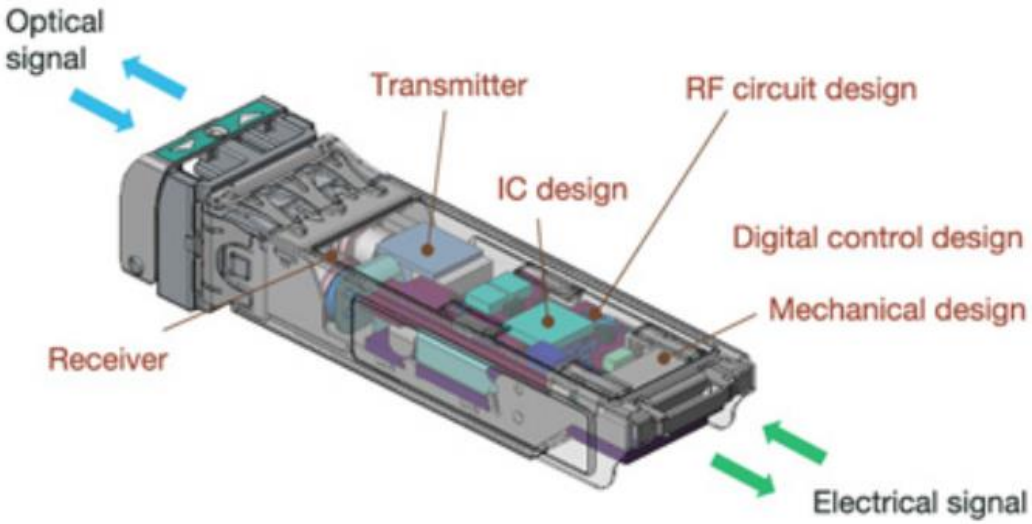
Optical transceivers.





Transceivers





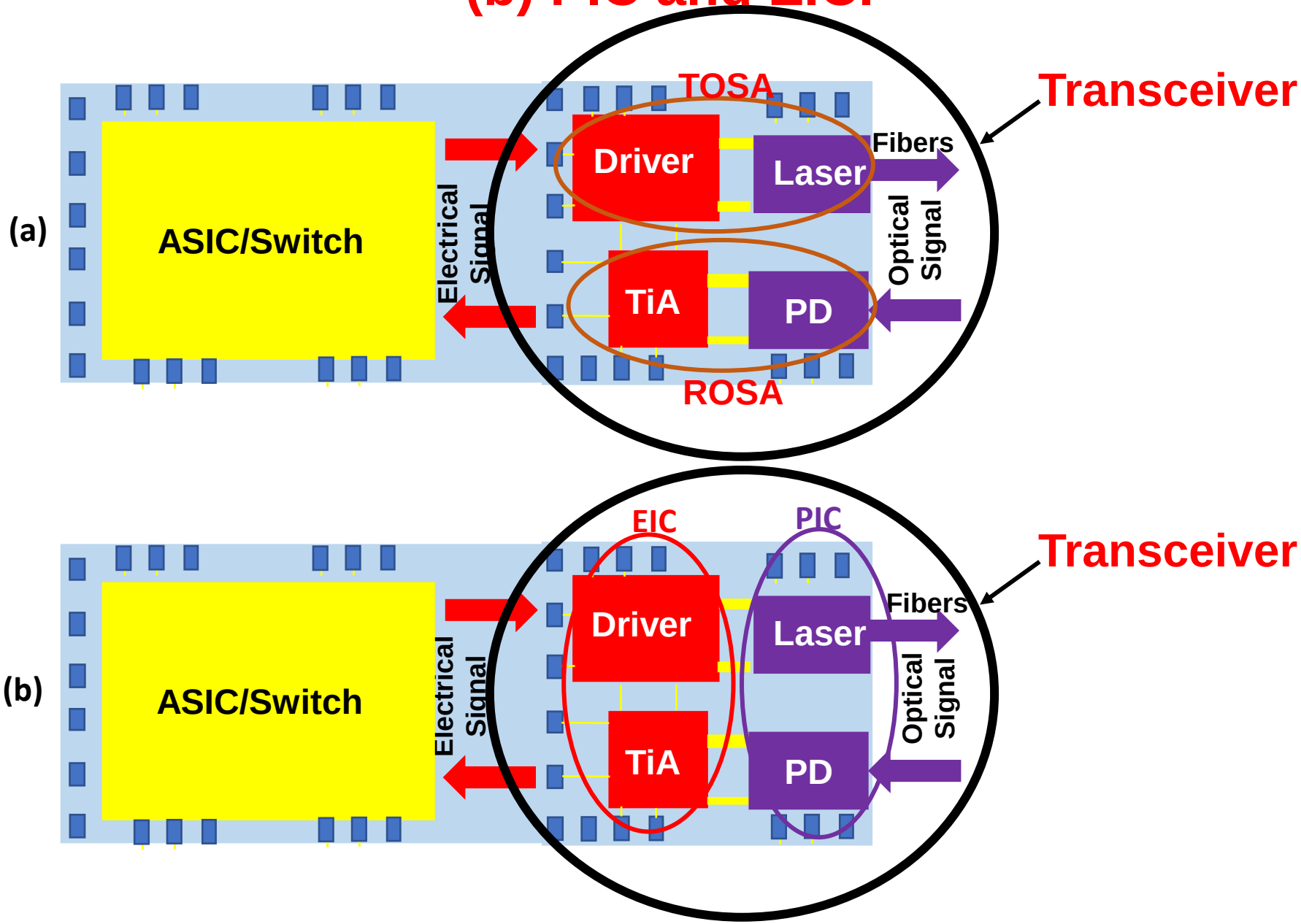
- **Optical Transceiver is a key component of an optical transmission system that permits coupling of the transmission medium with the active components of the chain, such as switches, routers - optical interfaces or any optical transport equipment.**

- **Transceiver is defining the process of converting electric signaling toward the optical transmission with the help of TOSA (Transmission Optical Sub Assembly) or Tx module and performing inverse action through the ROSA (Receiver Optical Sub Assembly) or Rx module.**

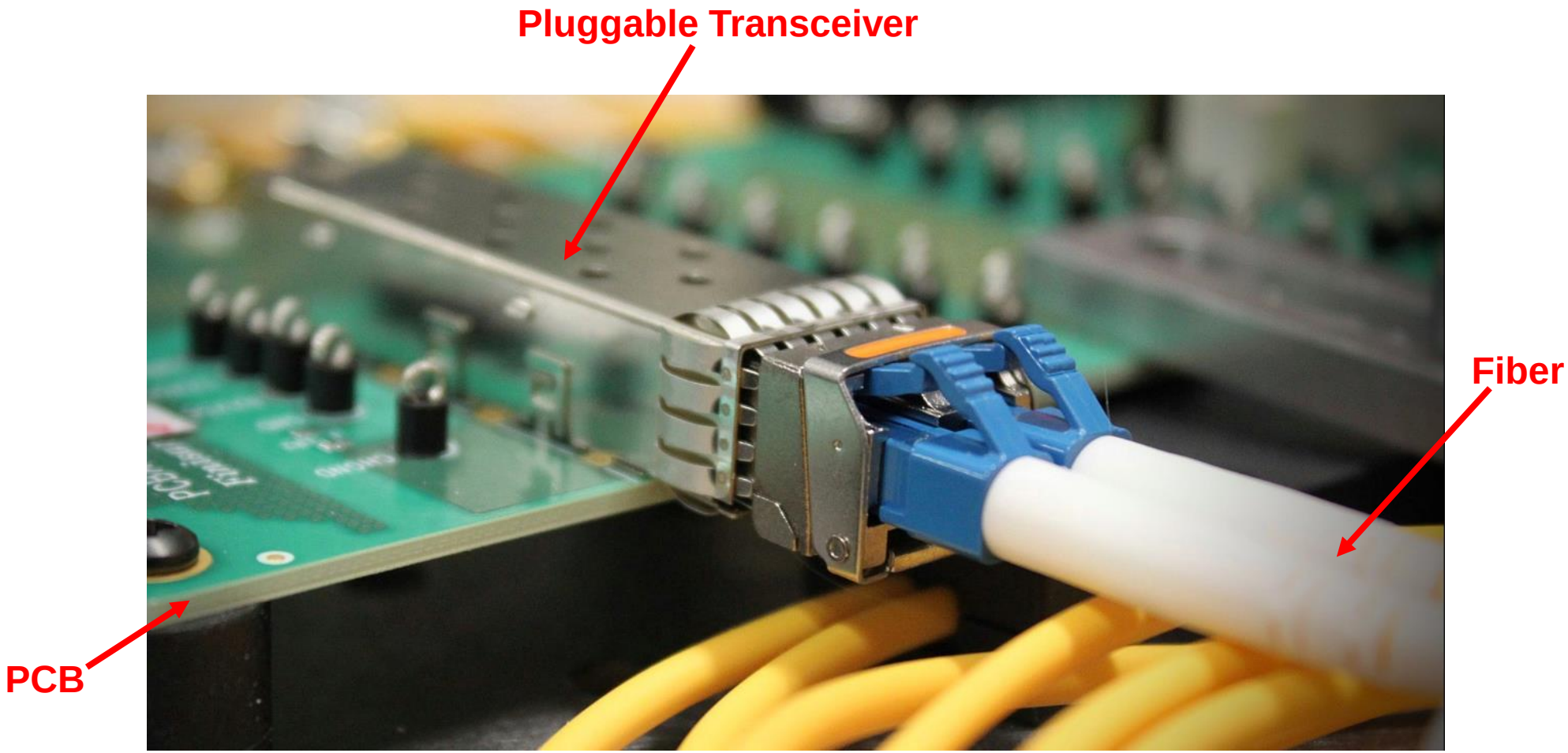
- **A TOSA contains a semiconductor laser diode (LD) and laser driver, while a ROSA contains a photodiode (PD), optical interface such as lens, TIA (transimpedance amplifier), and passive electrical interface.**

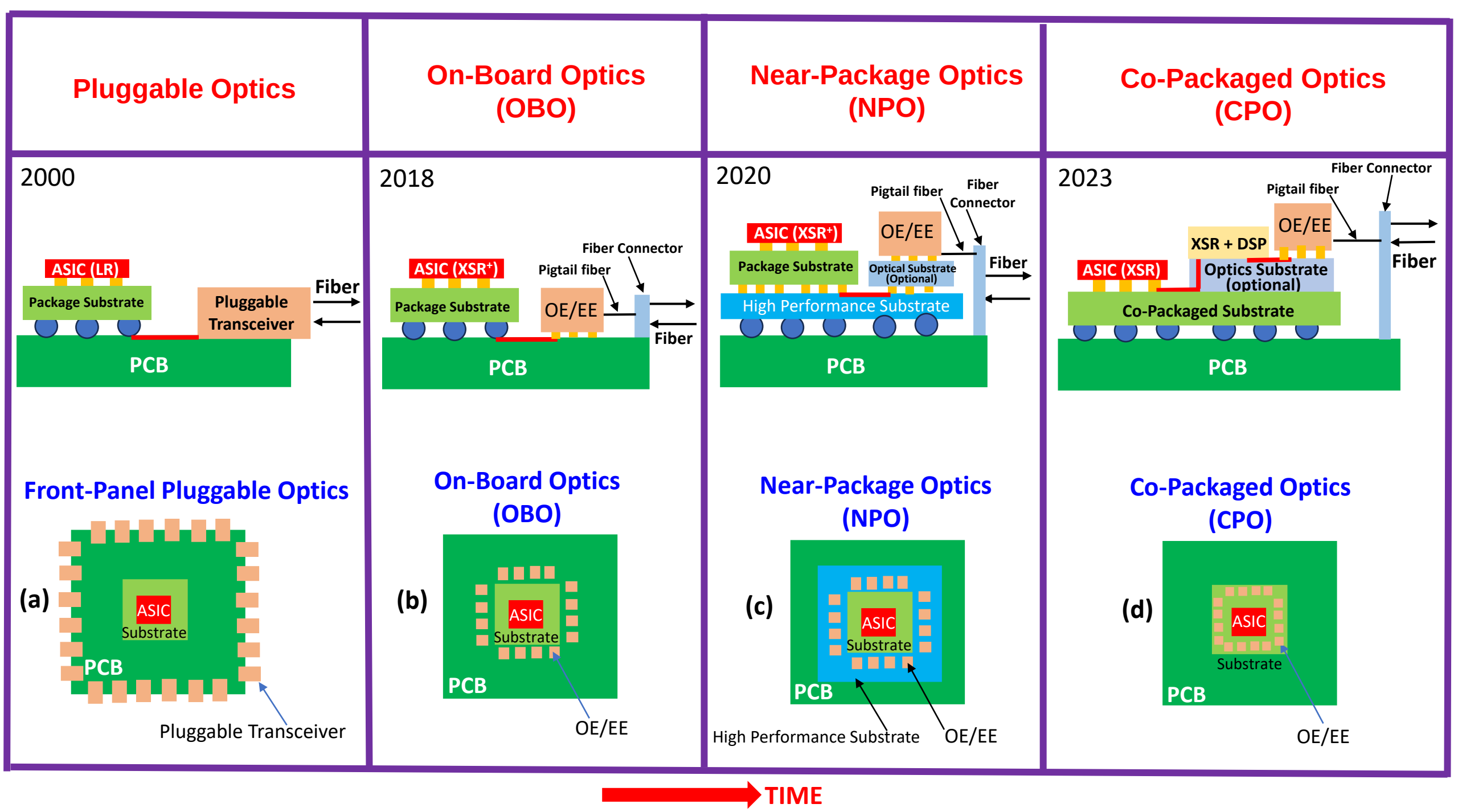
- **TOSA module converts the electrical signal to the optical transmission light that lands on the fiber. The ROSA is used to receive an optical signal from a fiber and convert it back into an electrical signal.**

Key components in an optical transceiver. (a) TOSA and ROSA. (b) PIC and EIC.

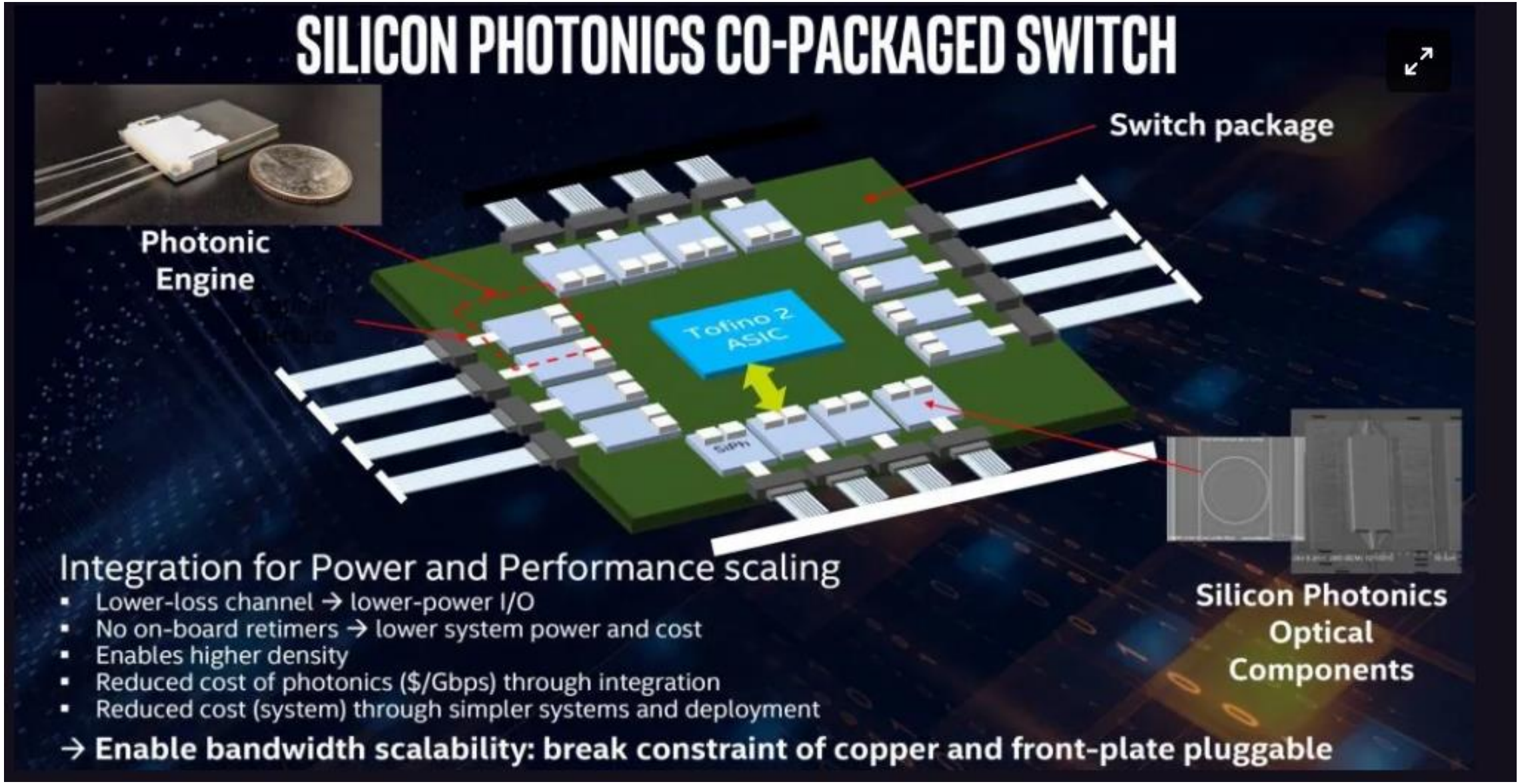


Pluggable Transceiver

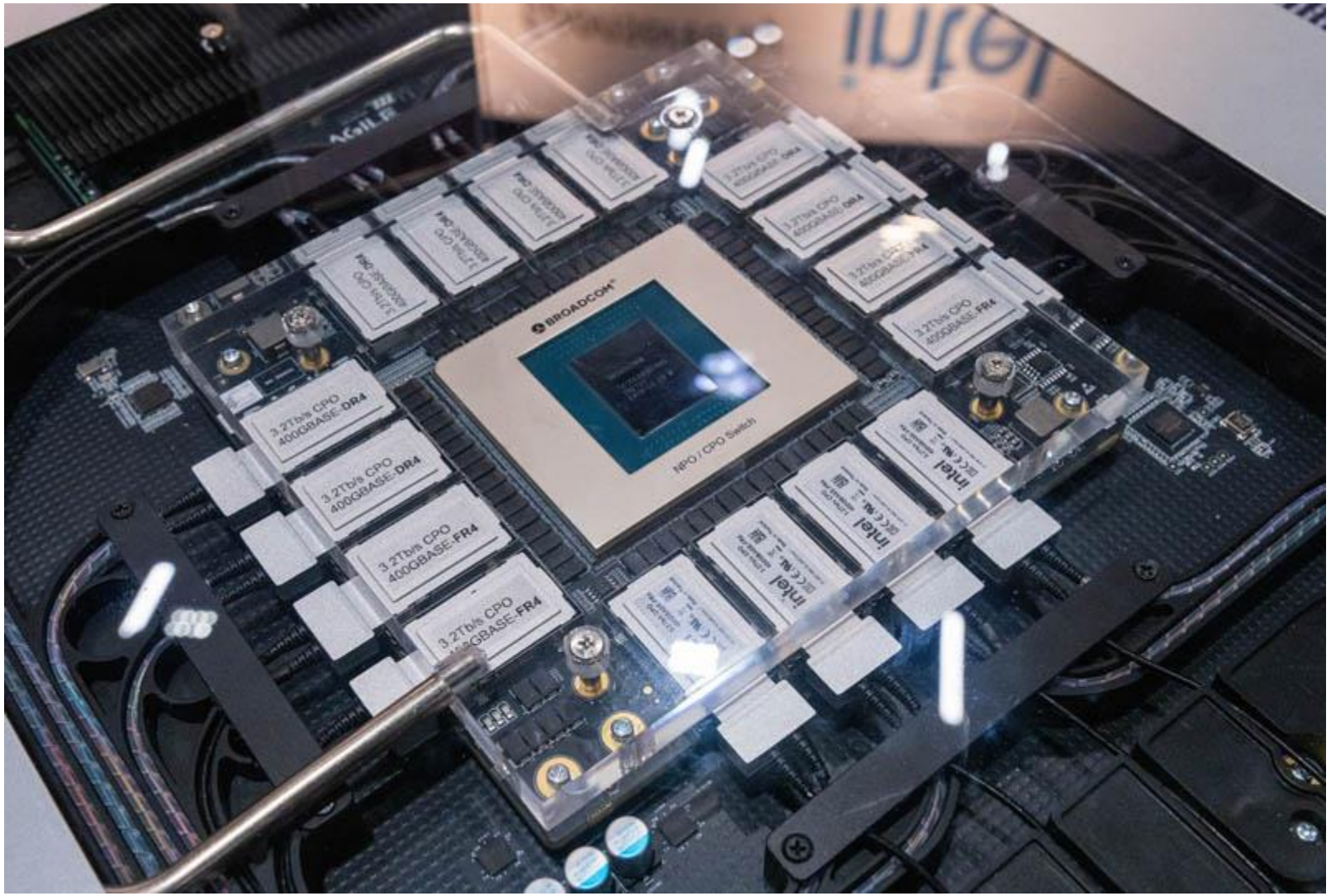



Pluggable Optics
On-Board Optics (OBO)
Near-Package Optics (NPO)
Co-Packaged Optics (CPO)
2000
ASIC (LR)
Package Substrate
Pluggable Transceiver
Fiber
PCB
2018
ASIC (XSR+)
Package Substrate
Pigtail fiber
Fiber Connector
OE/EE
Fiber
PCB
2020
ASIC (XSR+)
Package Substrate
Pigtail fiber
Fiber Connector
OE/EE
Optical Substrate (Optional)
Fiber
High Performance Substrate
PCB
2023
Fiber Connector
Pigtail fiber
OE/EE
XSR + DSP
ASIC (XSR)
Optics Substrate (optional)
Fiber
Co-Packaged Substrate
PCB
Front-Panel Pluggable Optics
(a)
ASIC
Substrate
PCB
Pluggable Transceiver
On-Board Optics (OBO)
(b)
ASIC
Substrate
PCB
OE/EE
Near-Package Optics (NPO)
(c)
ASIC
Substrate
PCB
High Performance Substrate
OE/EE
Co-Packaged Optics (CPO)
(d)
ASIC
Substrate
PCB
OE/EE
TIME

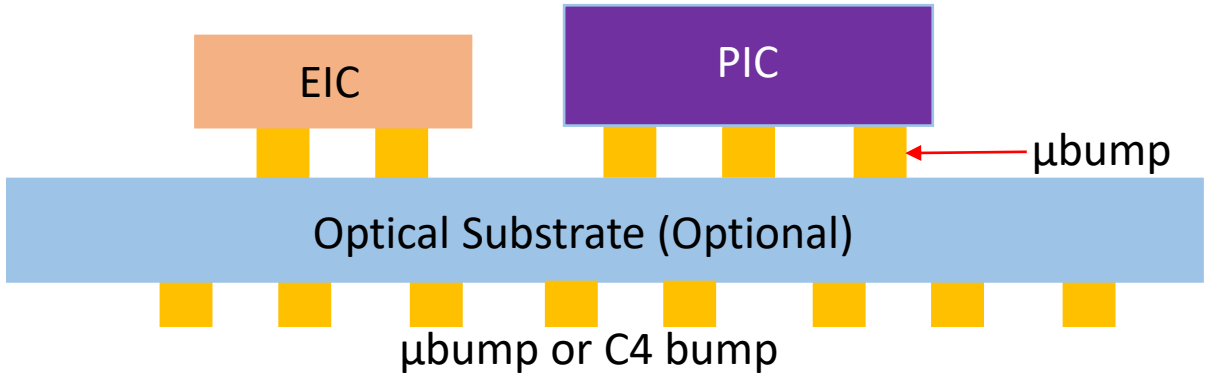
Intel’s co-packaged optics switch



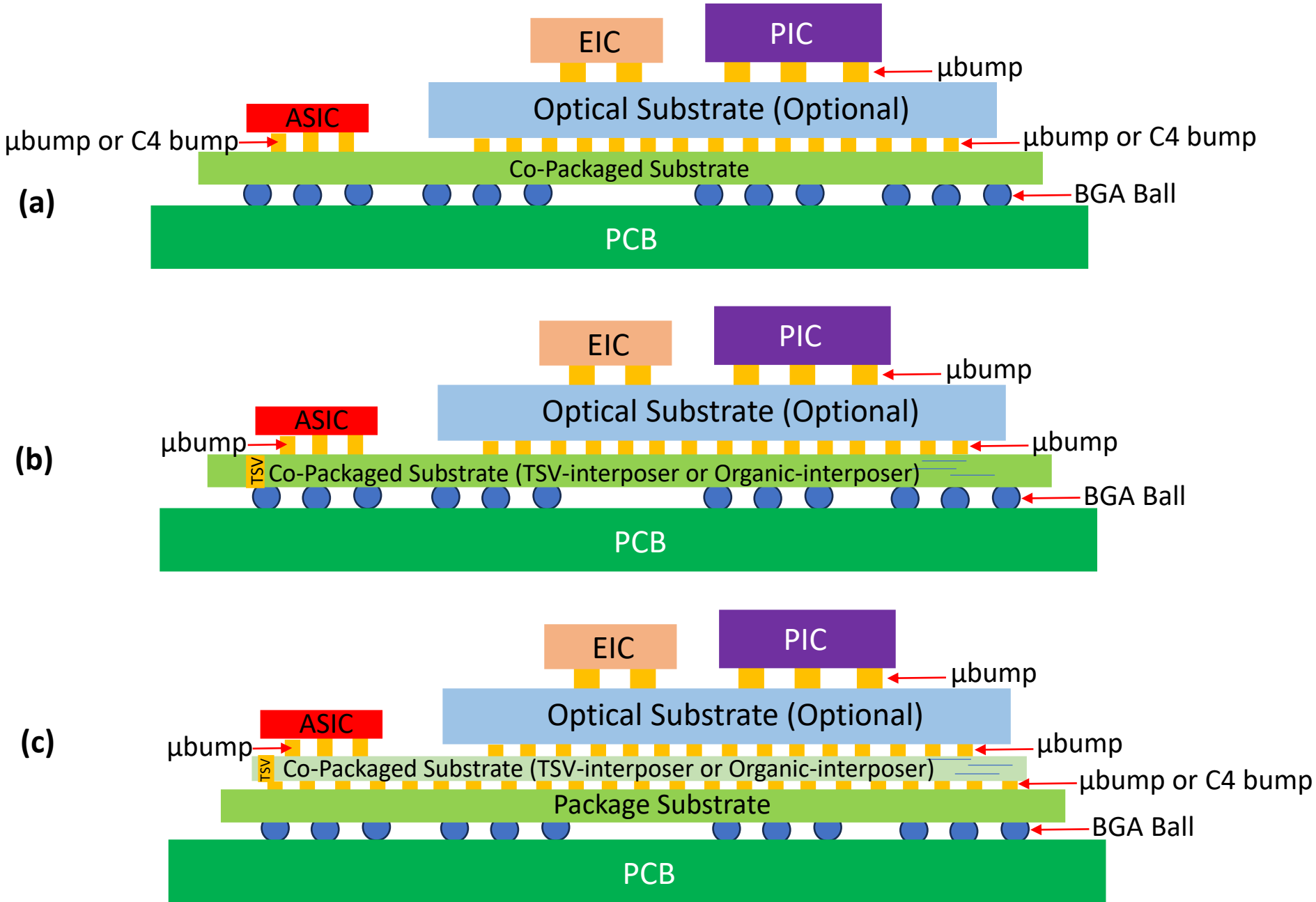
Broadcom’s co-packaged optics switch



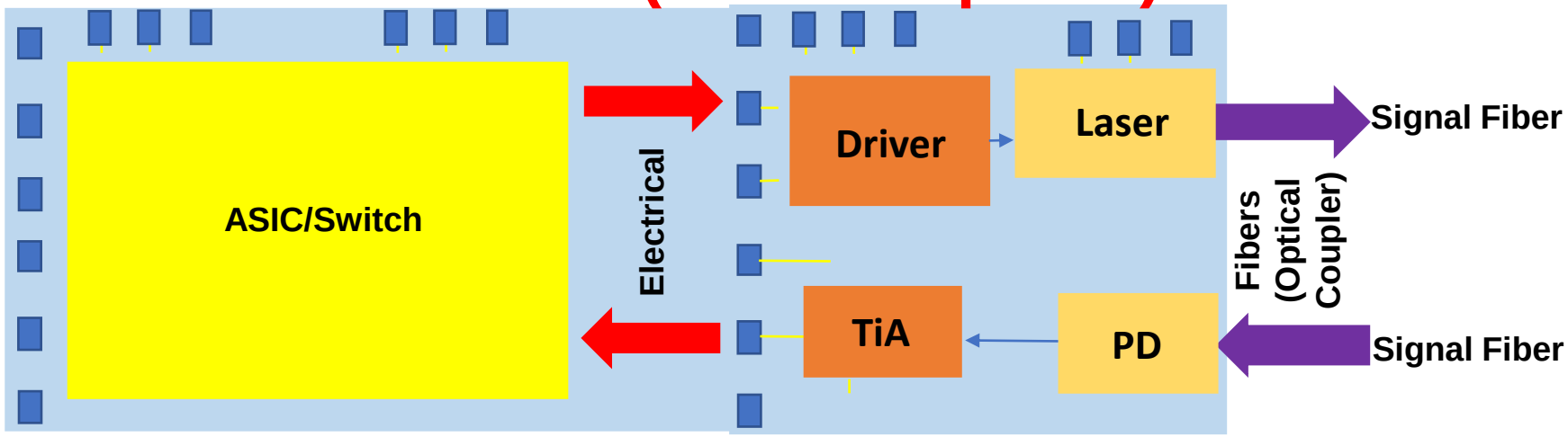
2D heterogeneous integration of EIC and PIC

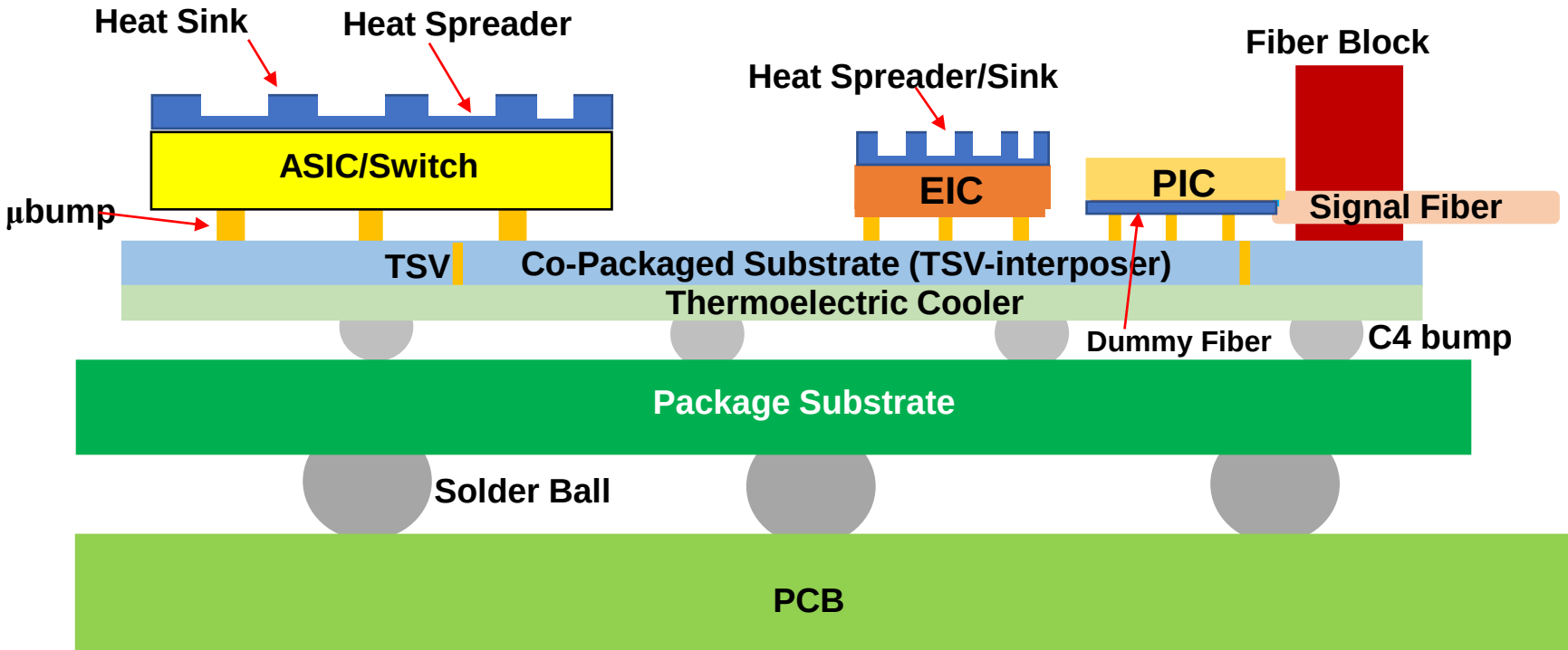


2D heterogeneous integration of ASIC, EIC and PIC. (a) On an ordinary co-packaged substrate. (b) On TSV-interposer or organicinterposer. (c) On TSV-interposer or organicinterposer and then on package substrate.

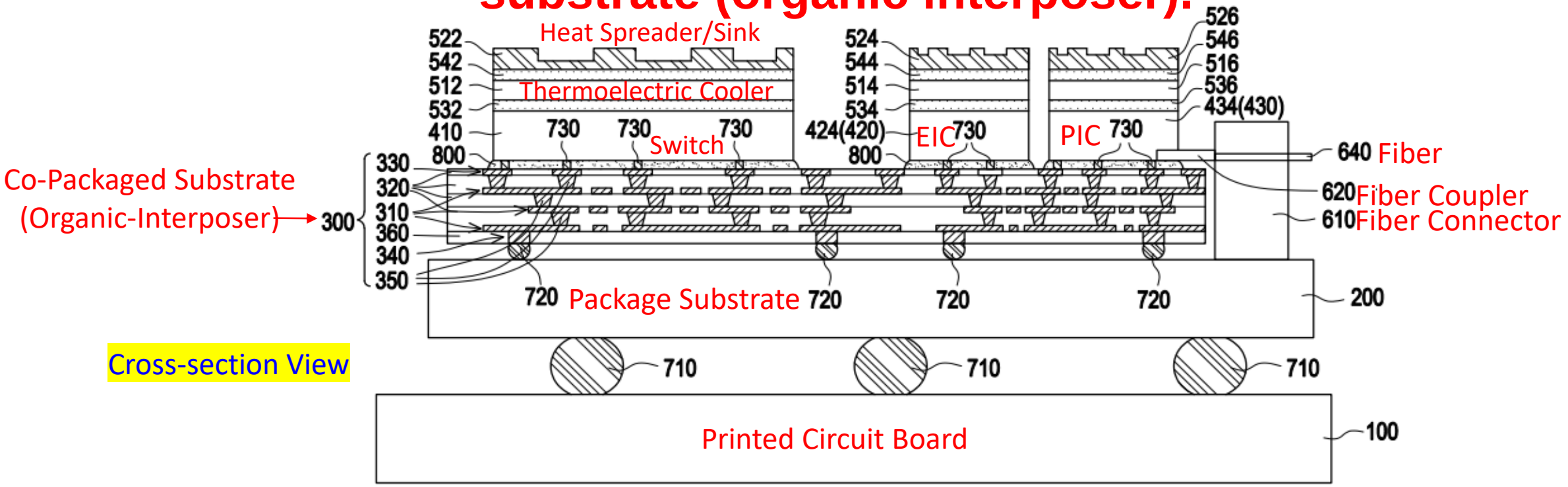


2D heterogeneous integration of ASIC, EIC and PIC on a co-packaged substrate (TSV-interposer)

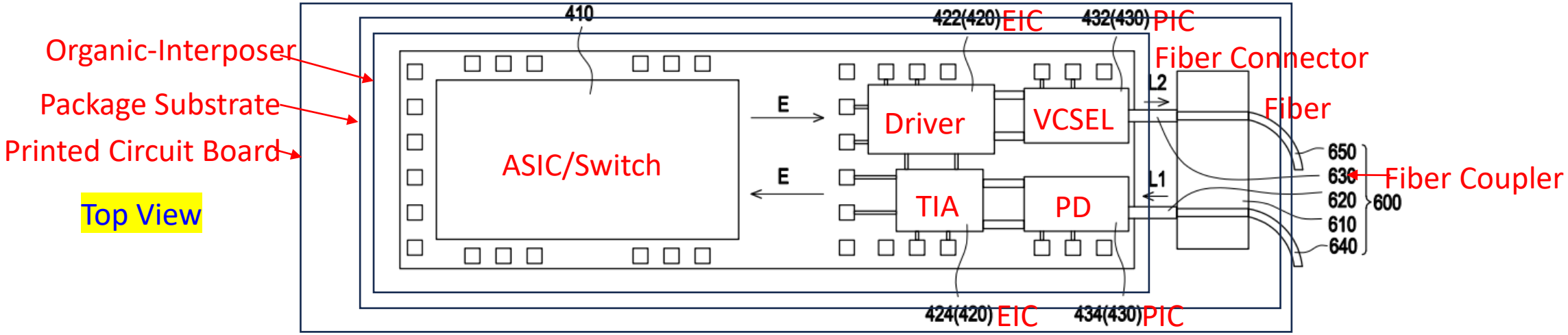




2D heterogeneous integration of ASIC, EIC and PIC on a co-packaged substrate (organic interposer).

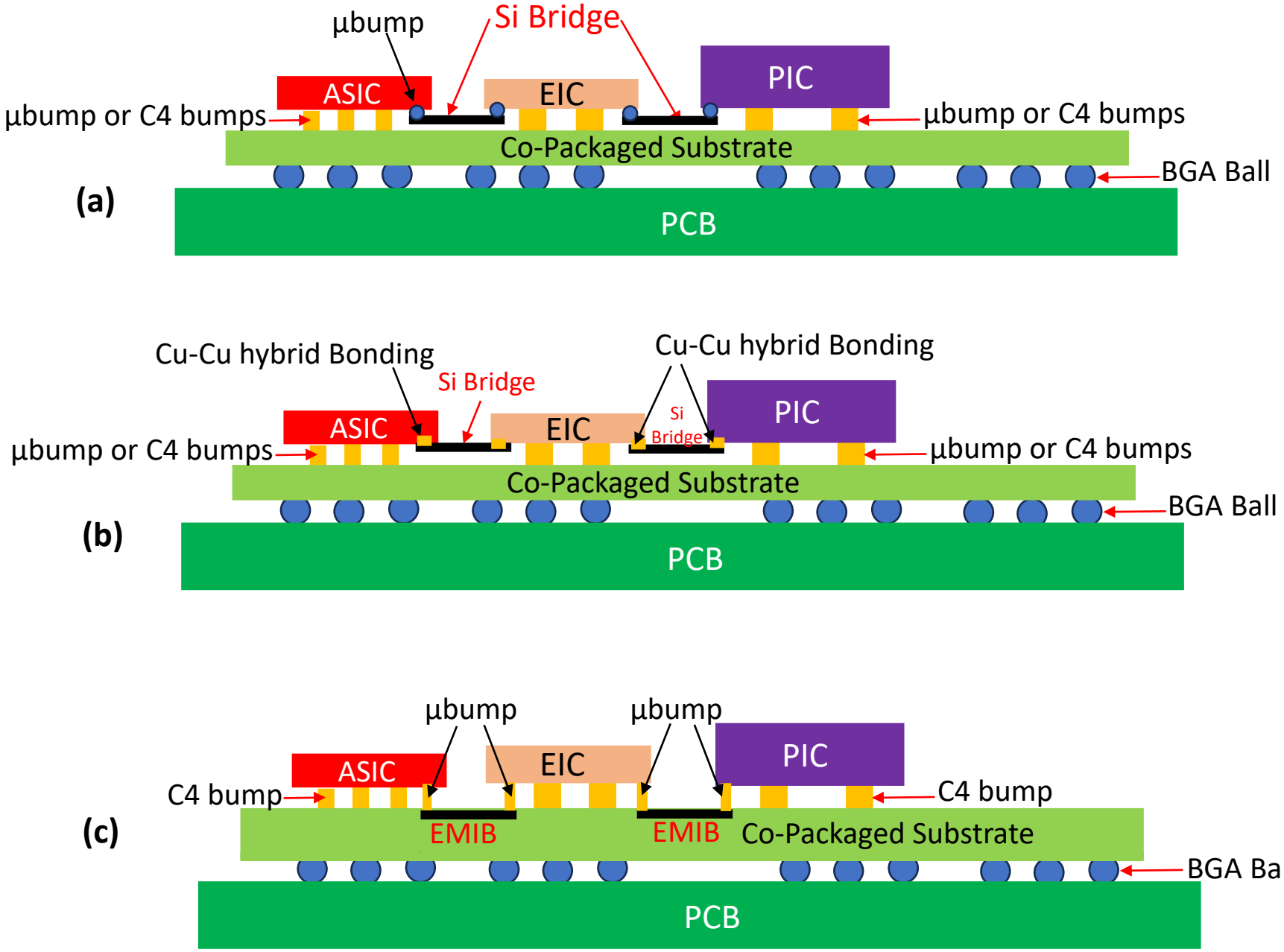


Cross-section View

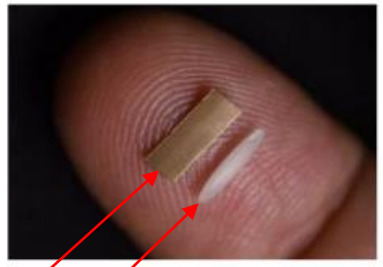


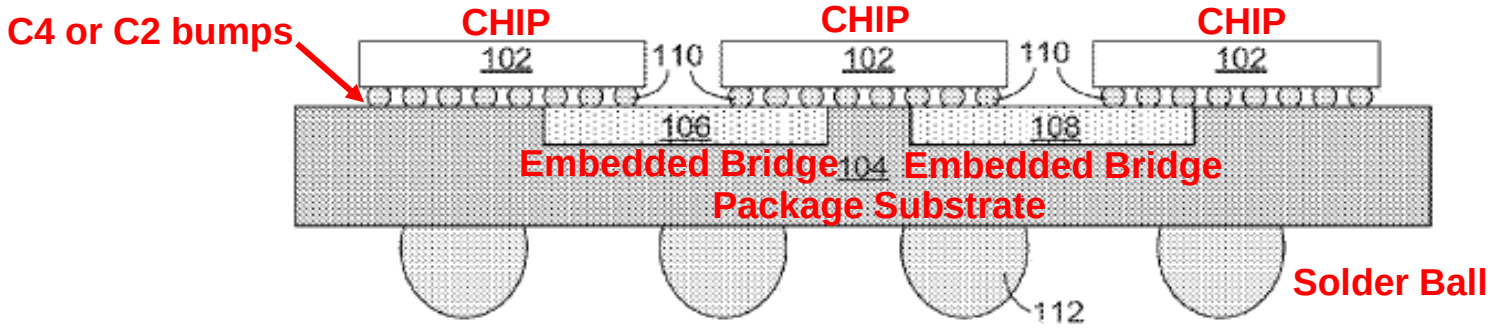
Top View

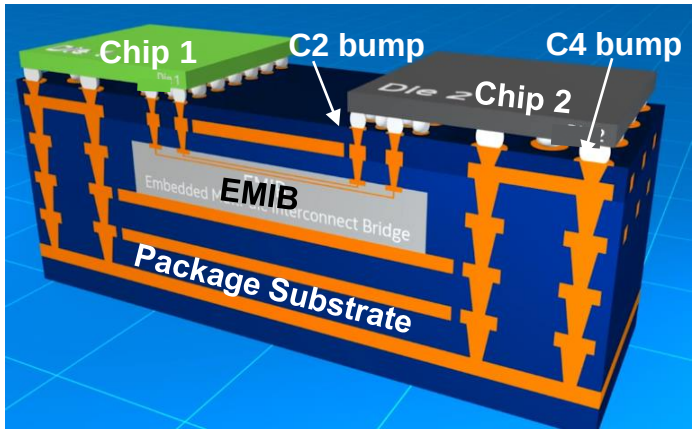
2D heterogeneous integration of ASIC, EIC and PIC with silicon bridges on a copackaged substrate. (a) Bridge with µbumps. (b) Bridge with hybrid bonding. (c) EMIB.

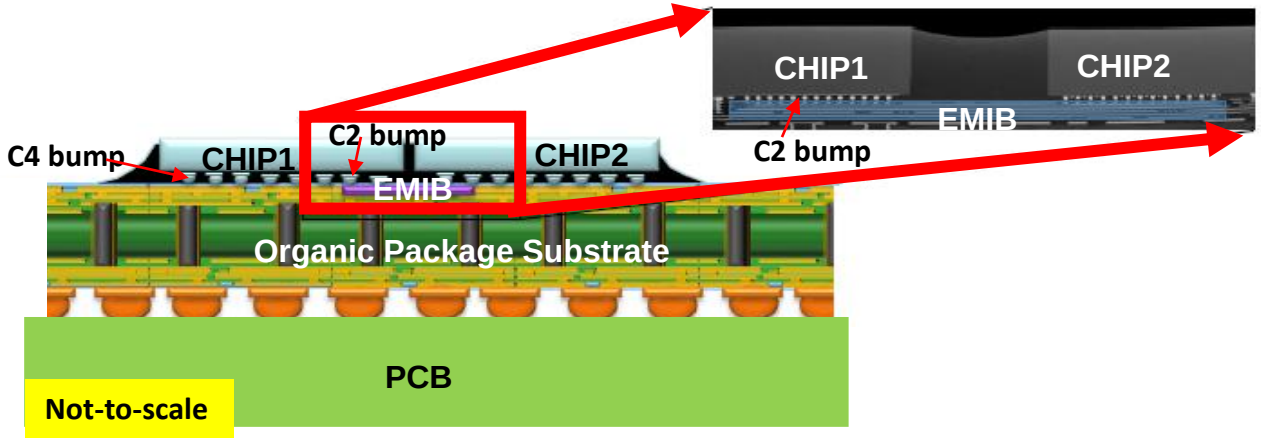


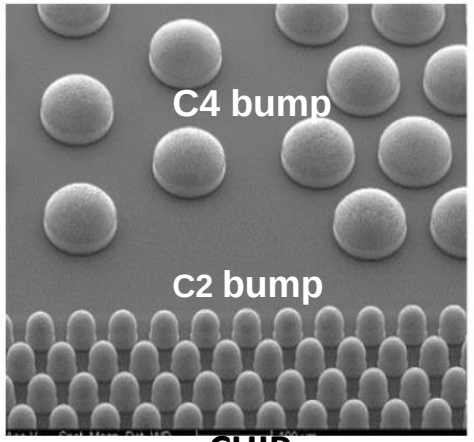
Intel's EMIB (Embedded Multi-die Interconnect Bridge)

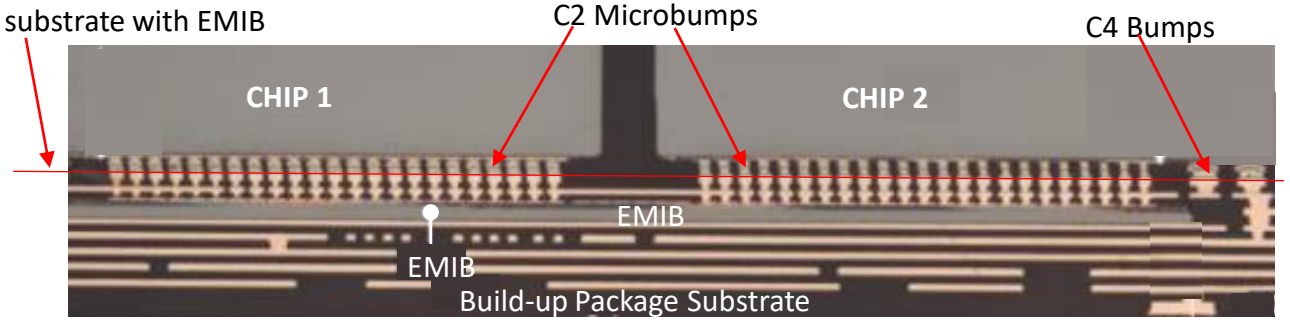








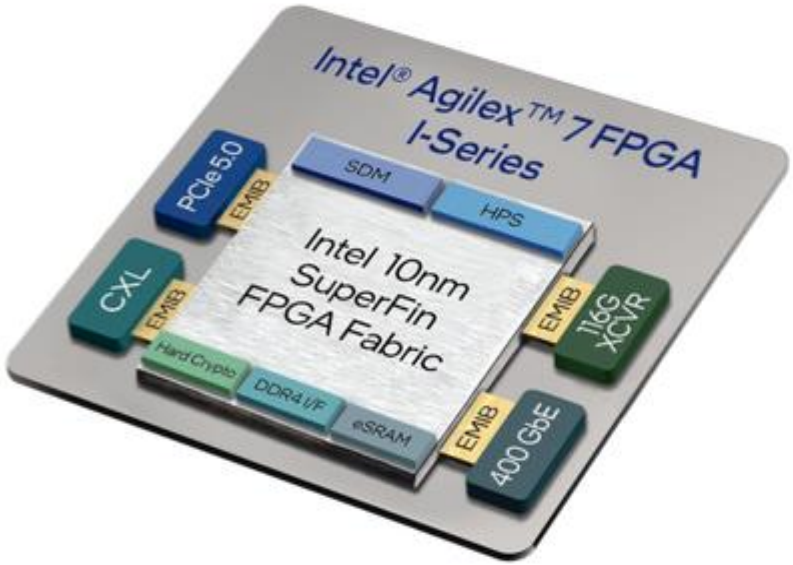


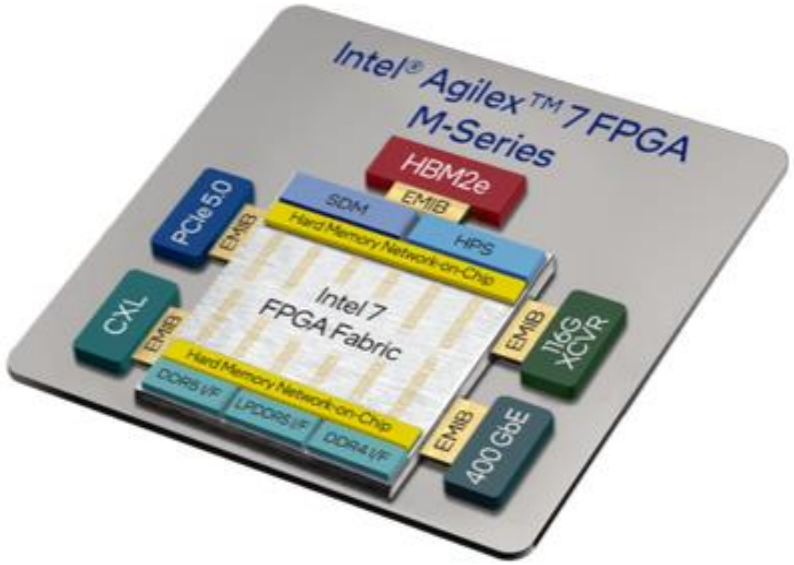


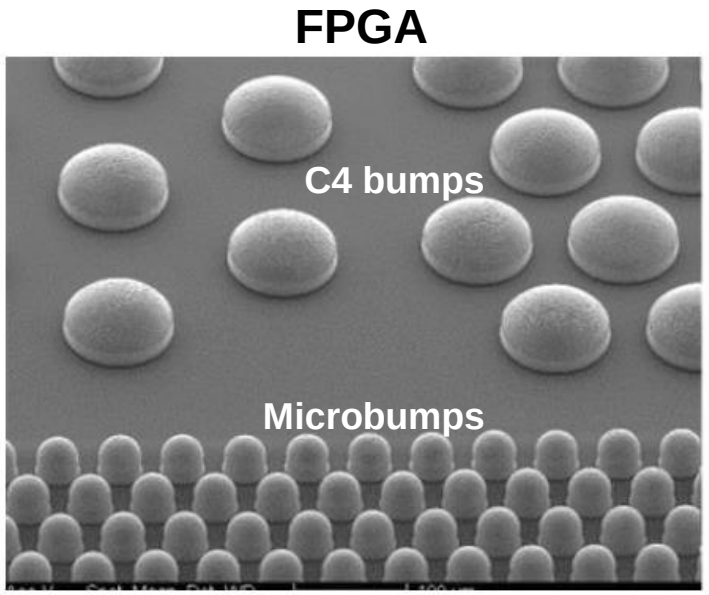
ECTC2016

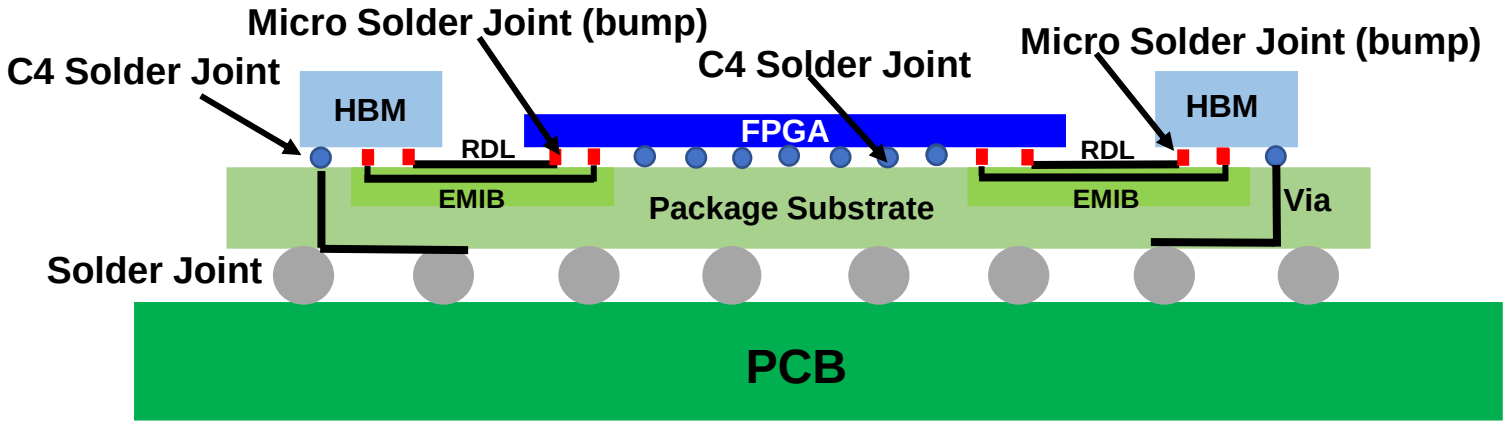
The objective of EMIB is to replace TSV-Interposer (2.5D IC Integration)

Intel's FPGA (Agilex) with EMIB



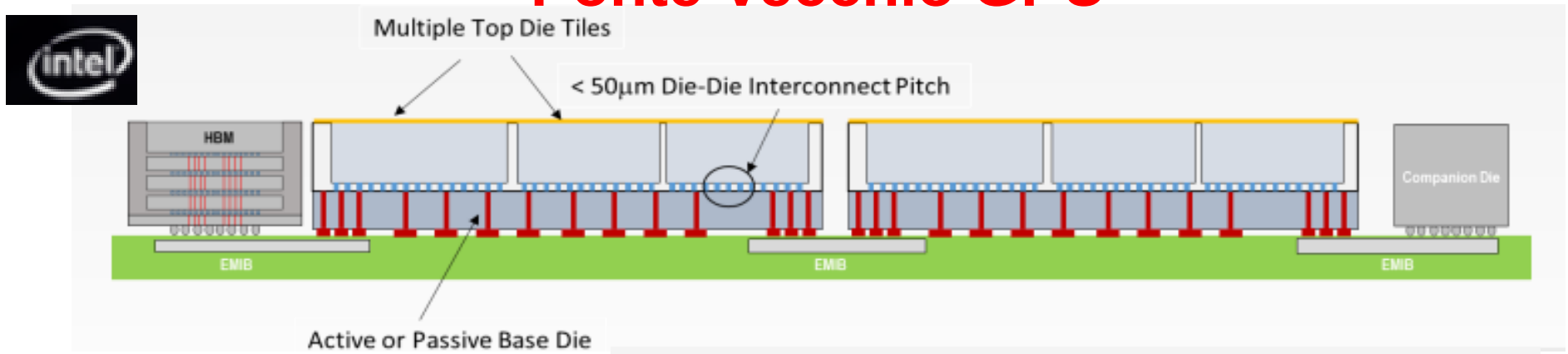


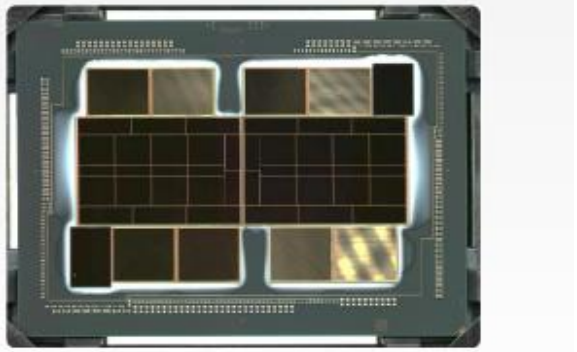


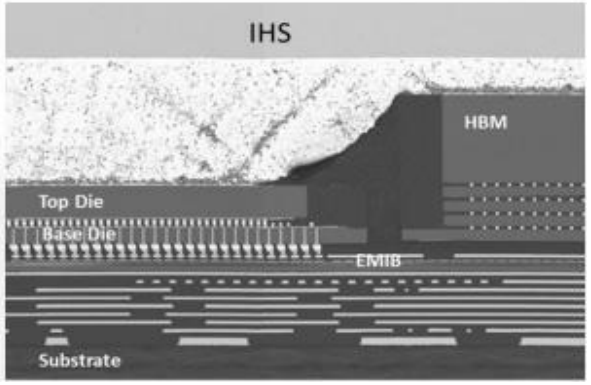


Shipped in September 2019

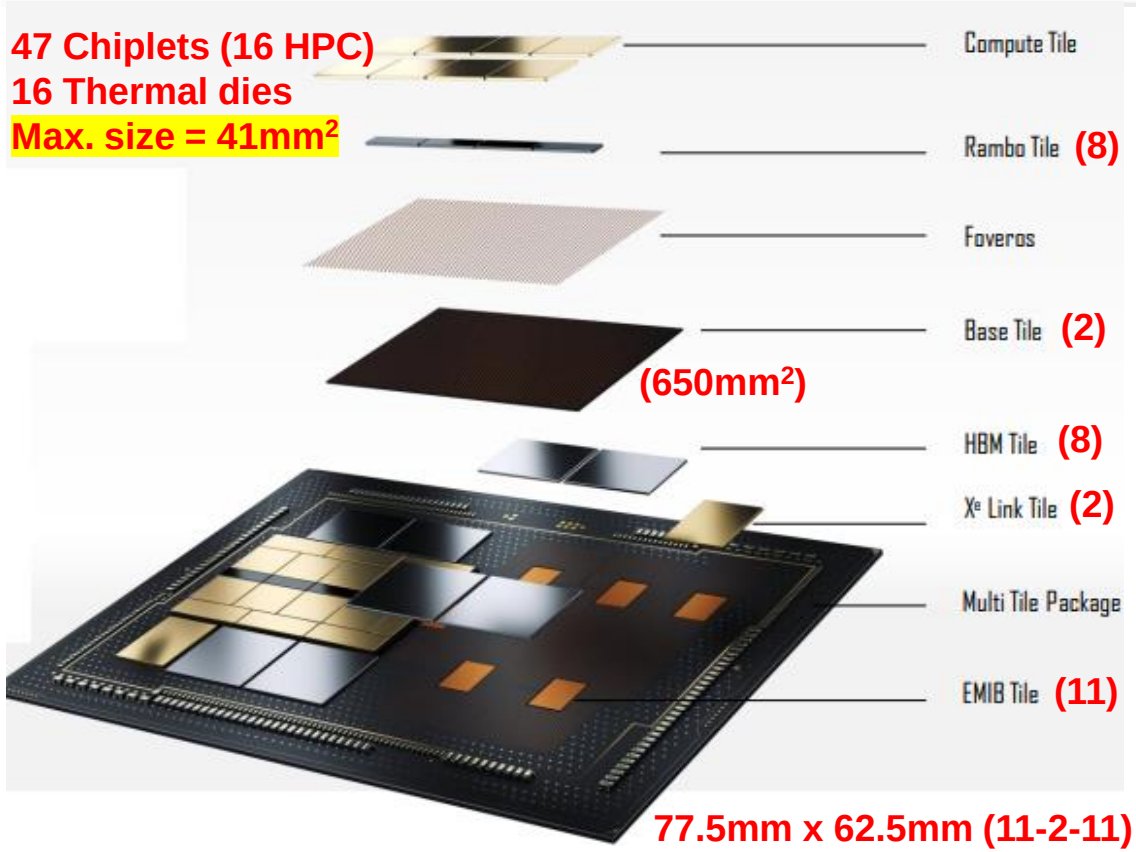
Intel's Chiplet Design and Heterogeneous Integration Packaging:- Ponte Vecchio GPU







- 47 Chiplets (16 HPC)
- 16 Thermal dies
- Max. size = 41mm²



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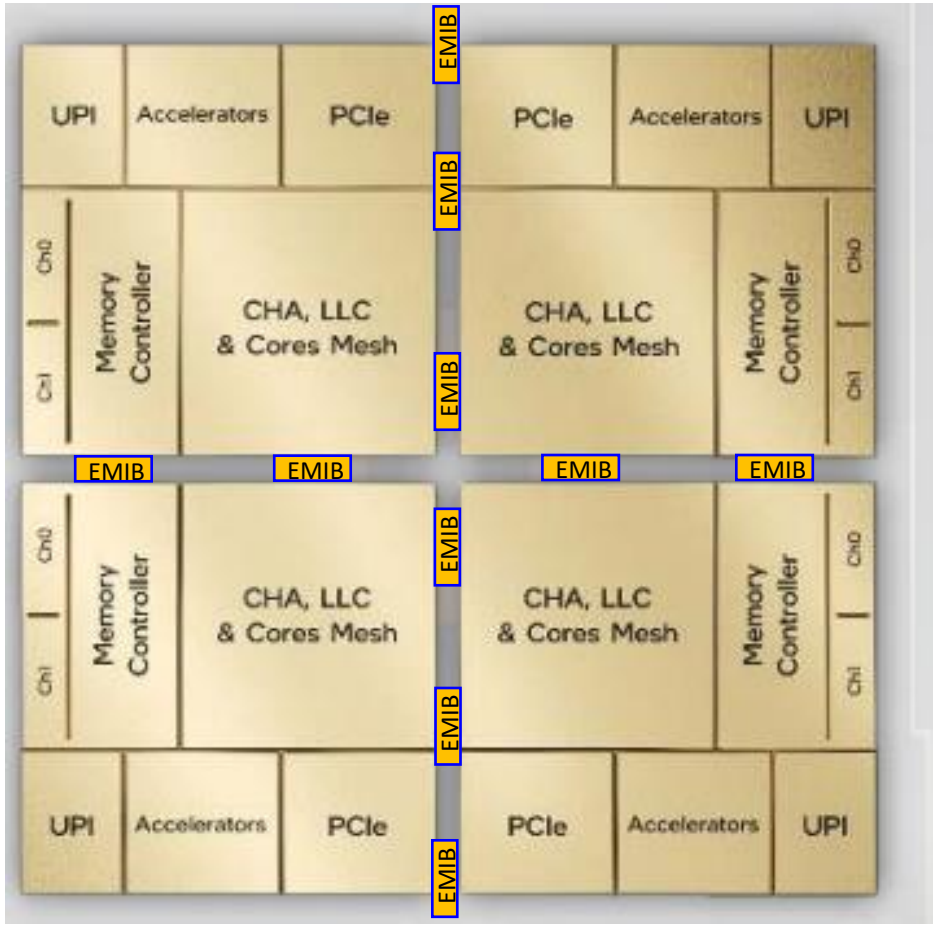
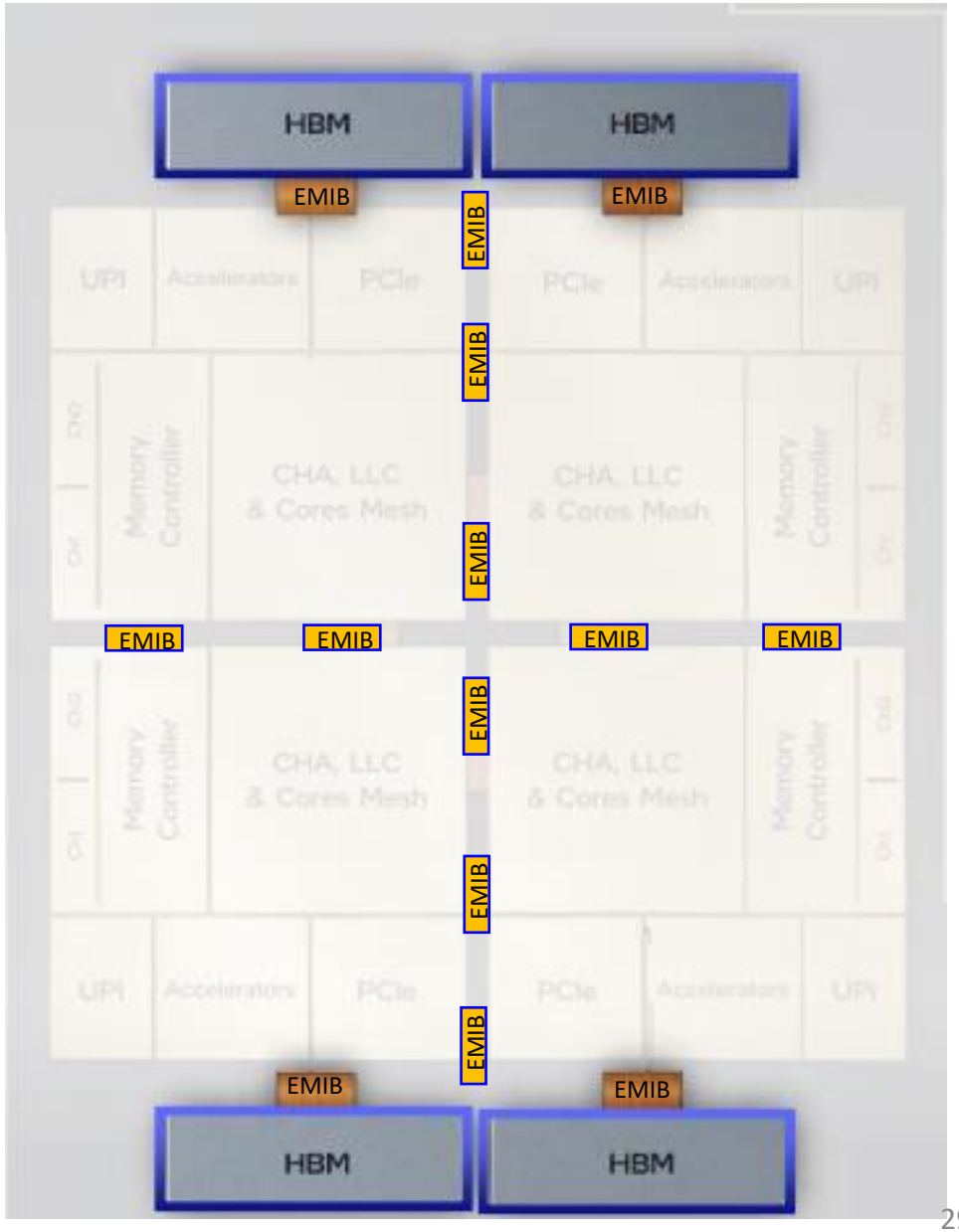
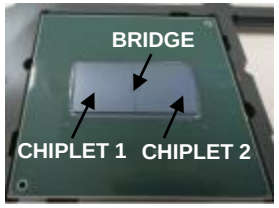
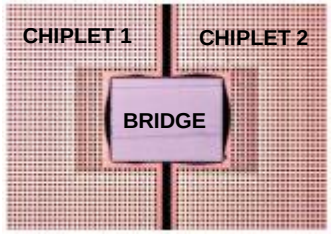
EMIB (Embedded Multi-Die Interconnect Bridge) for Sapphire Rapids

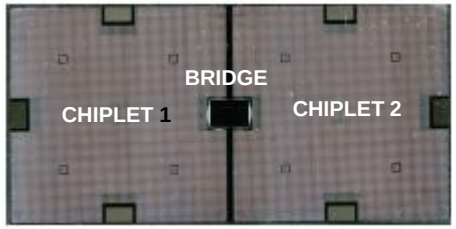


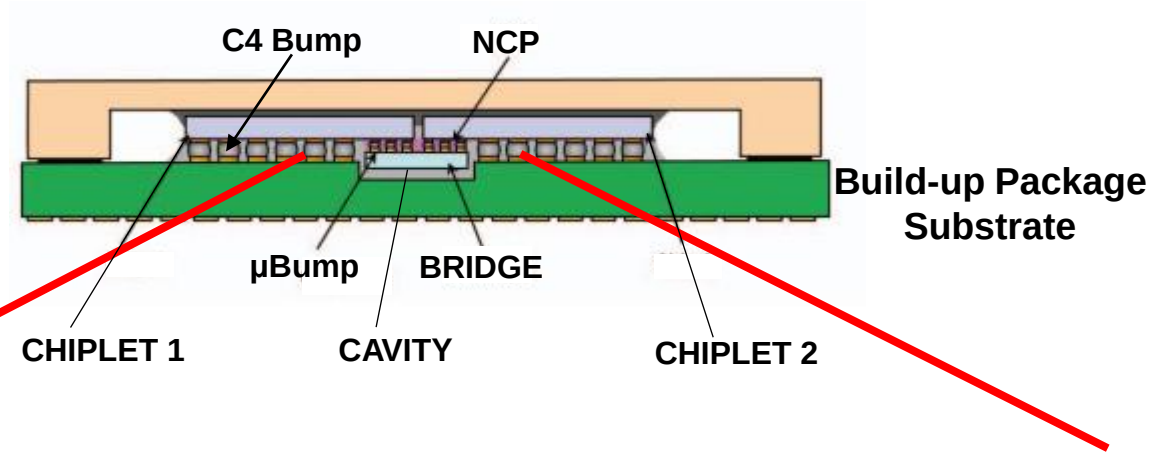


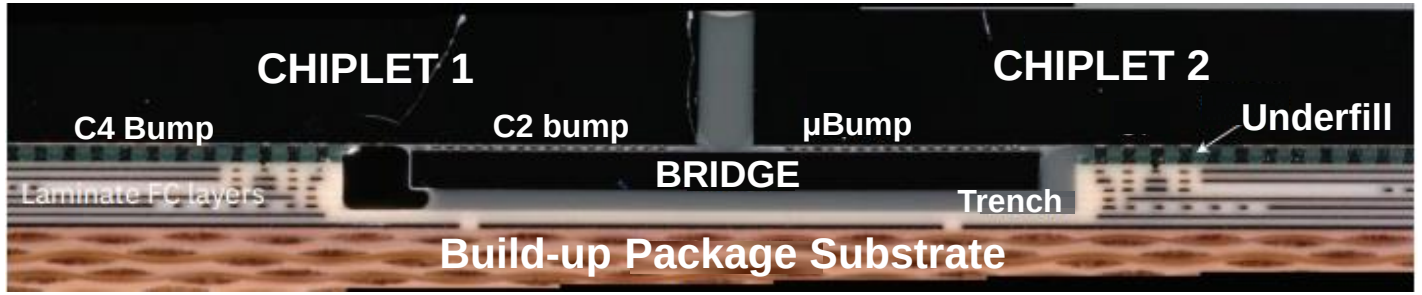
IBM's Direct Bonded Heterogeneous Integration (DBHi) Si Bridge

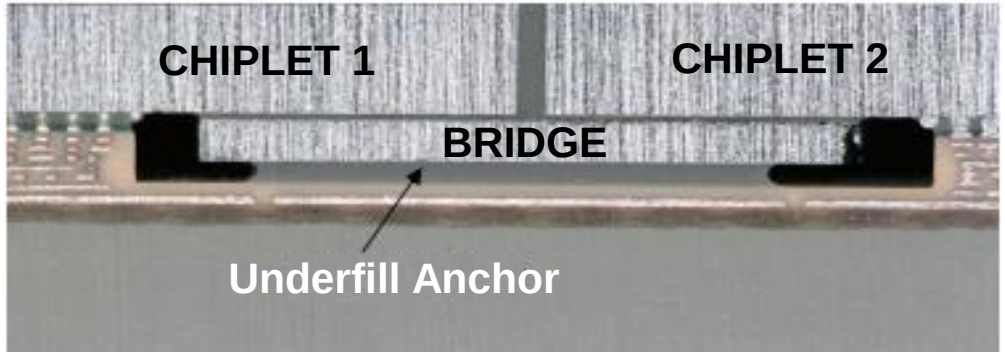


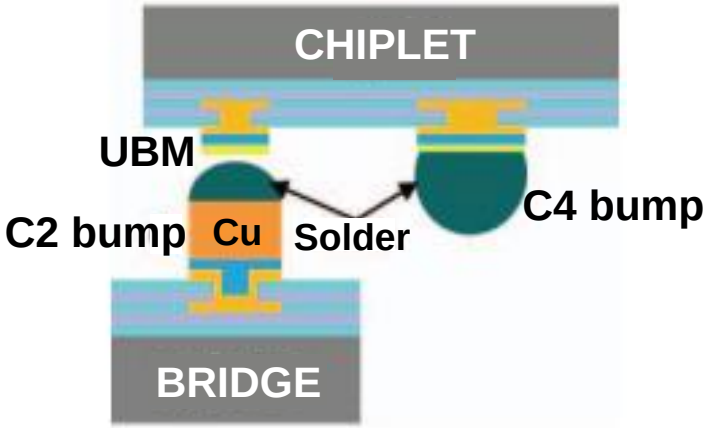












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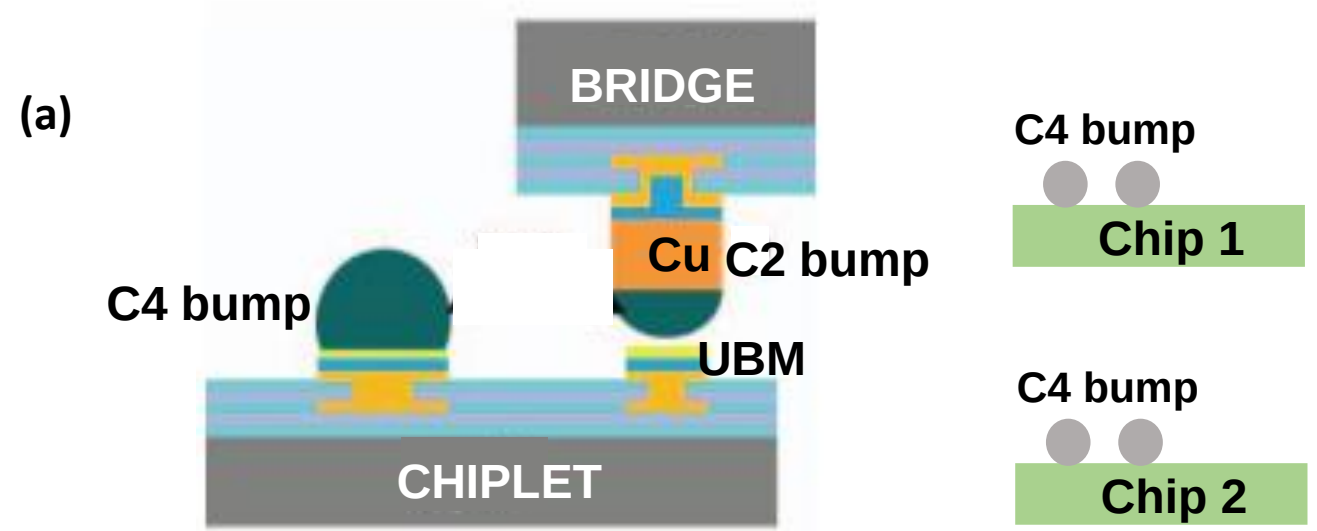
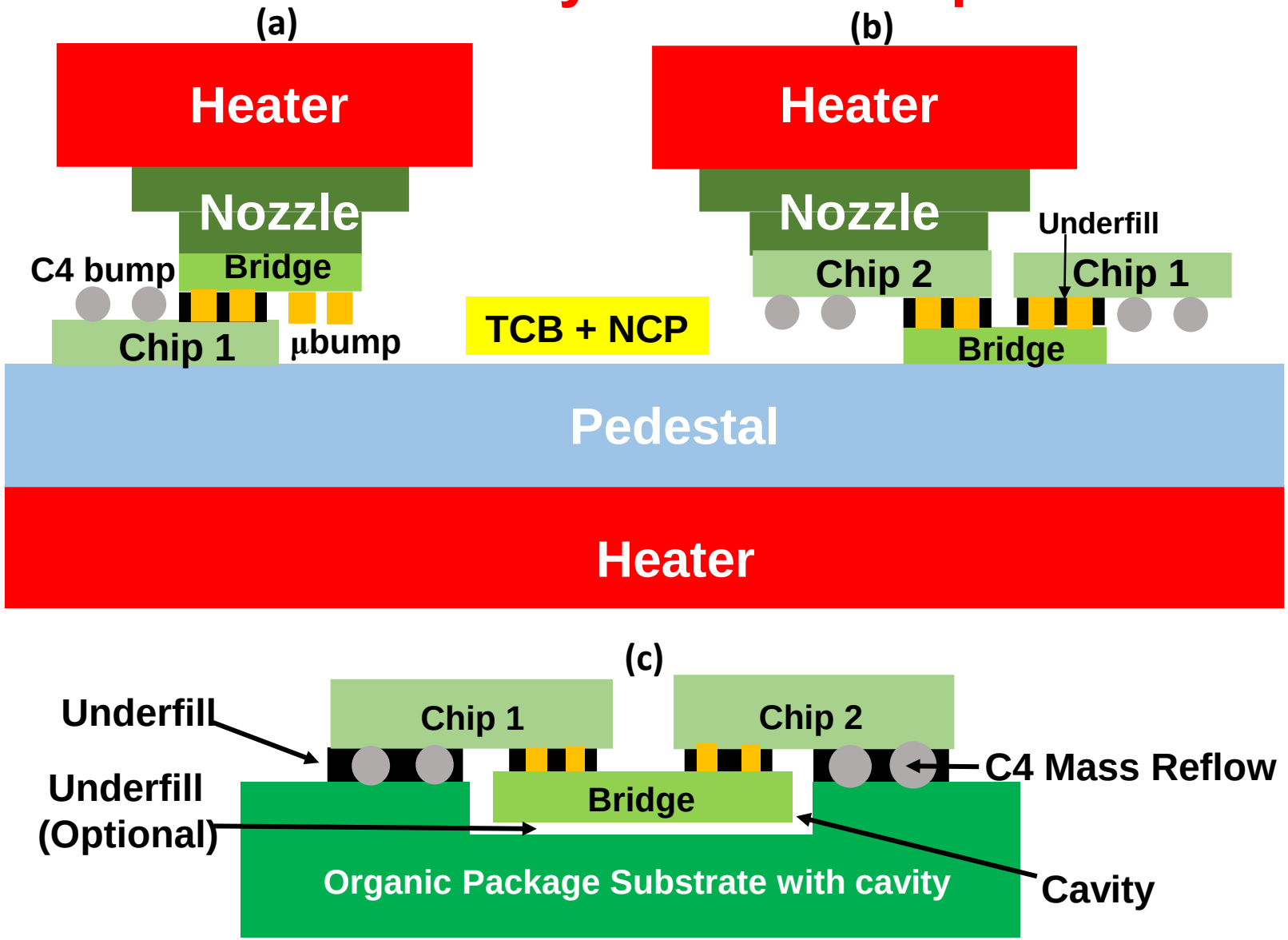
IBM's DBHi Key Process Steps



a) C2 bumps on the bridge, while C4 bumps on the chiplet.
b) Ordinary build-up package substrate with a cavity.

IBM's DBHi Key Process Steps



a) TCB/NCP of bridge die with C2 µbumps on Chip 1 with C4 bumps (NCP becomes the underfill).
b) TCB/NCP of Chip 2 with C2 µbumps on the bridge with the bonded Chip 1.
c) Place the module (bridge + Chip 1 + Chip 2) on the substrate and mass reflow the C4 bumps. Apply the capillary underfill to the C4 bumps.

Direct Bonded Heterogeneous Integration (DBHi): Surface bridge approach for die tiling

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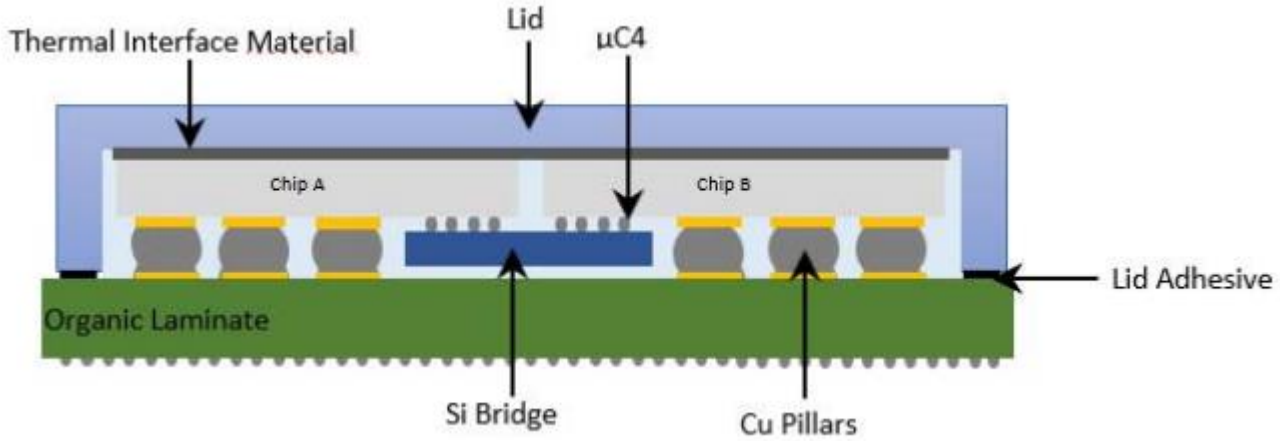
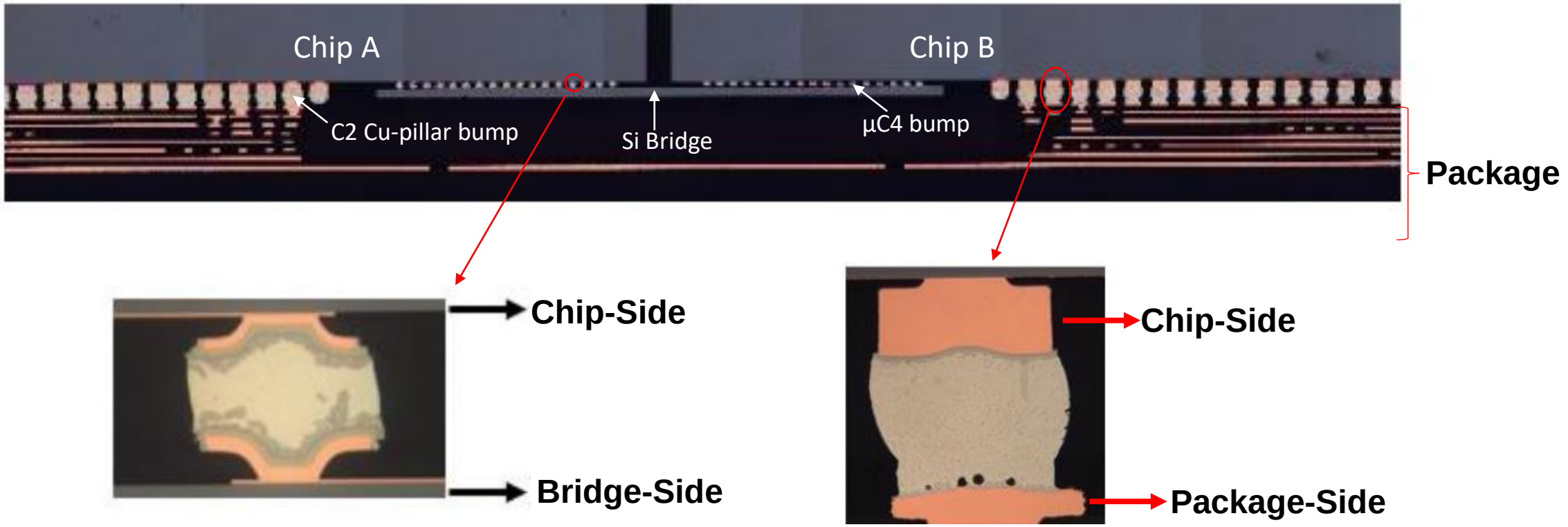


Improvements of IBM's DBHi

- The Si-bridge is not in the cavity of a package substrate
- Thickness of Si Bridge = 60 - 70μm
- Dimensions of Bridge = 3.5mm × 2.5mm x 60-70μm
- Nonconductive paste → Solder and Reflow



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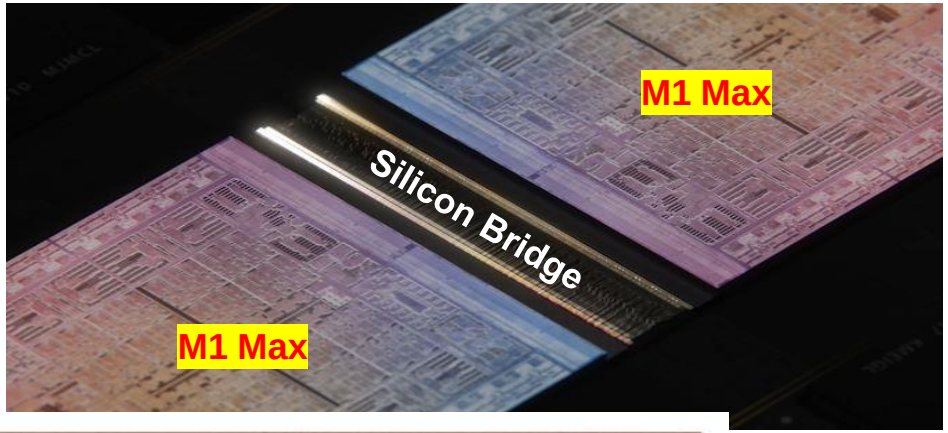
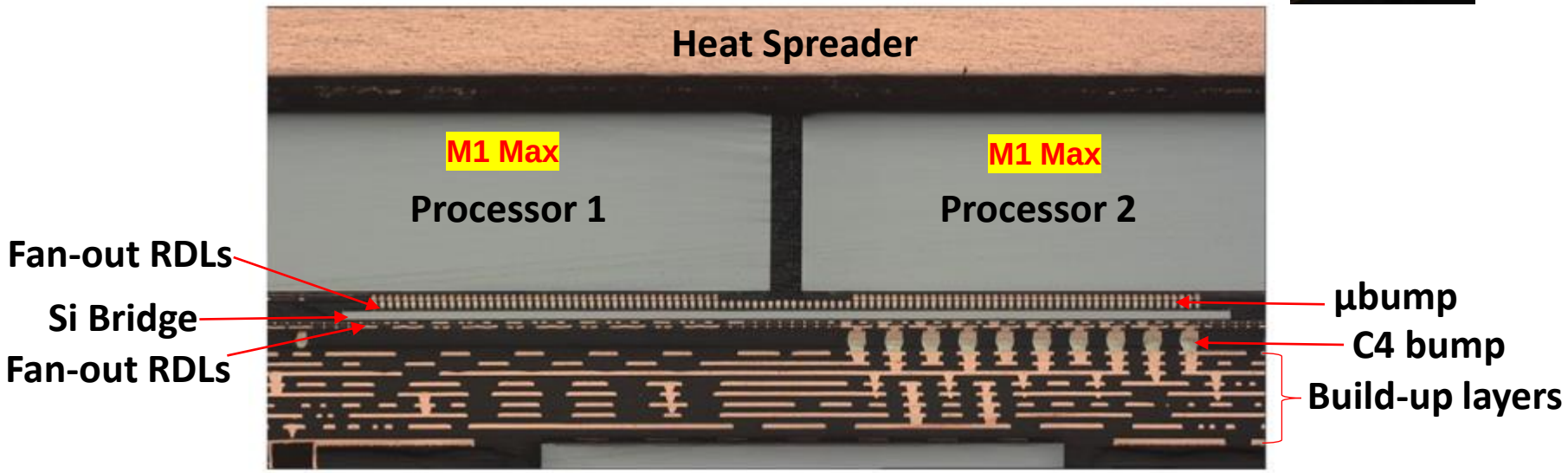
Apple's UltraFusion
(M1 Ultra = M1 Max + M1 Max + Si Bridge)

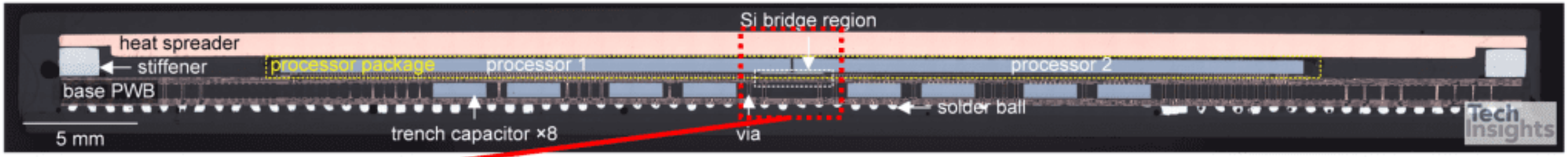


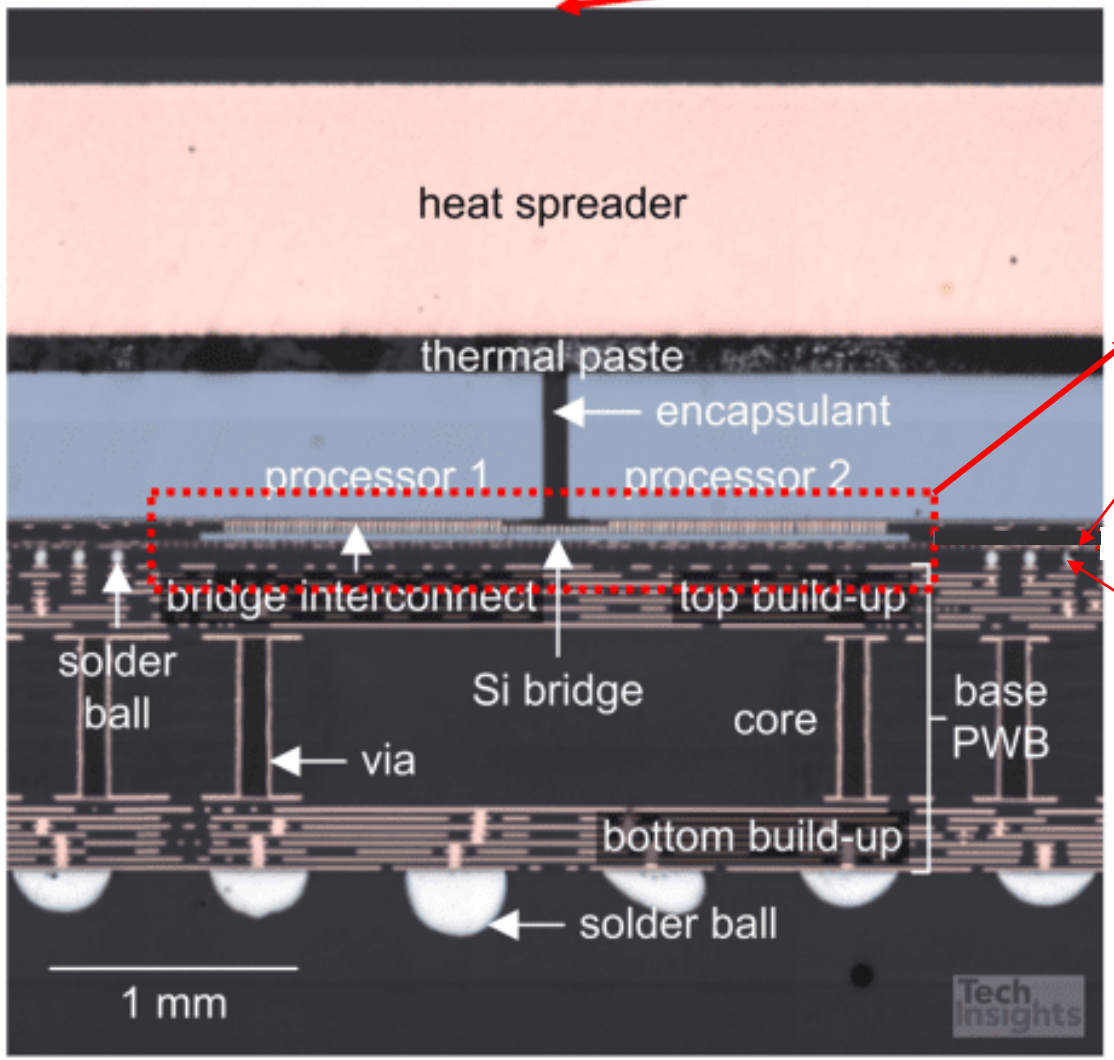


UltraFusion — Apple's innovative packaging architecture that interconnects the die of two M1 Max chips to create a system on a chip (SoC) with unprecedented levels of performance and capabilities. TSMC assembled the package with silicon bridge what TSMC called LSI (local silicon interconnect).

Shipped in March 2022

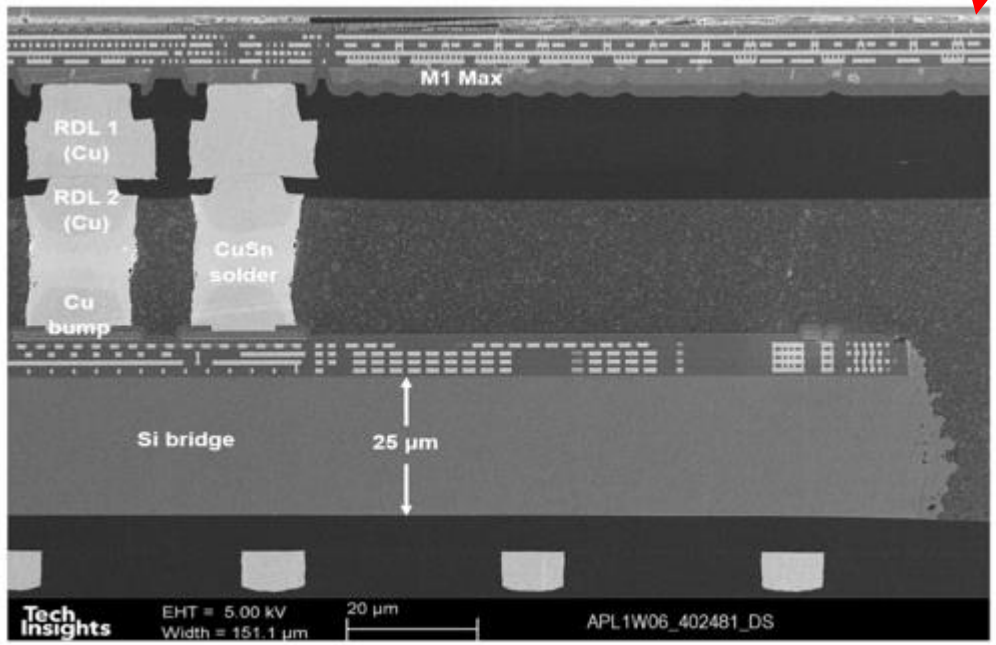
Apple's UltraFusion with TSMC's LSI (Bridge) Shipped in March 2022



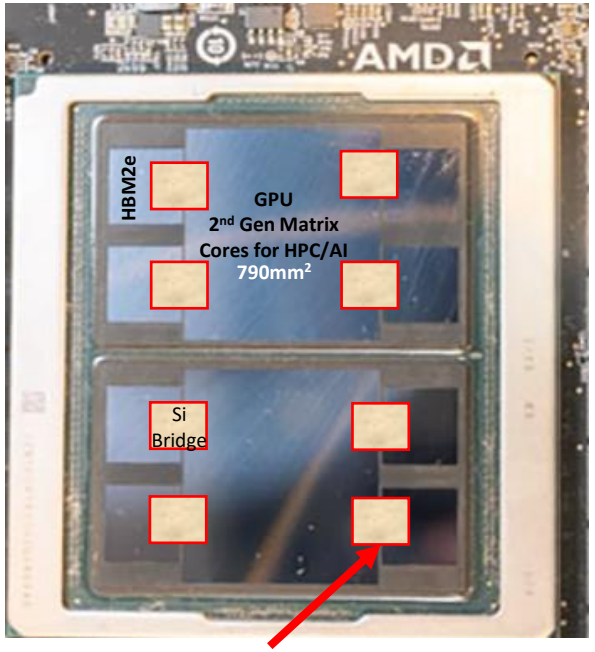


RDLs

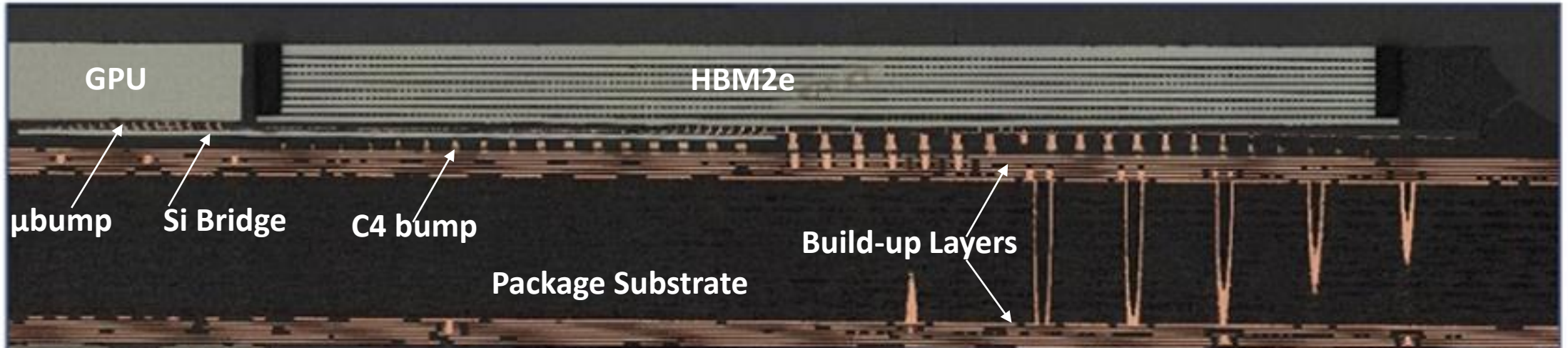
C4 bump



AMD's Instinct MI250X Compute Accelerator (GPU/HBM2 Interfaced with Si Bridge on Fan-out RDLs)

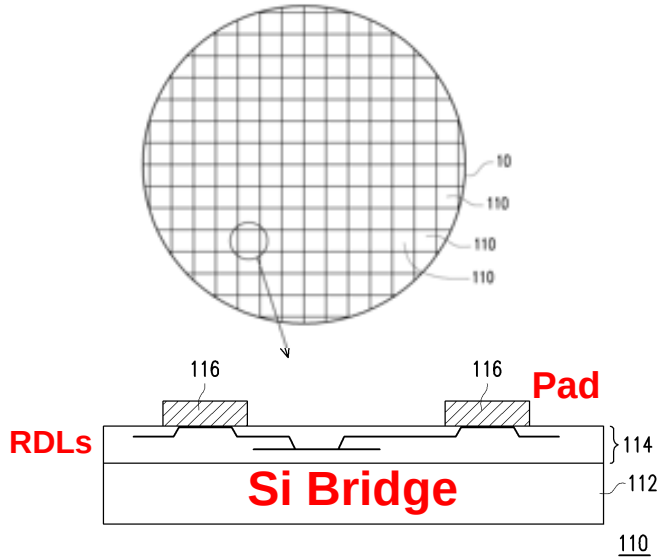


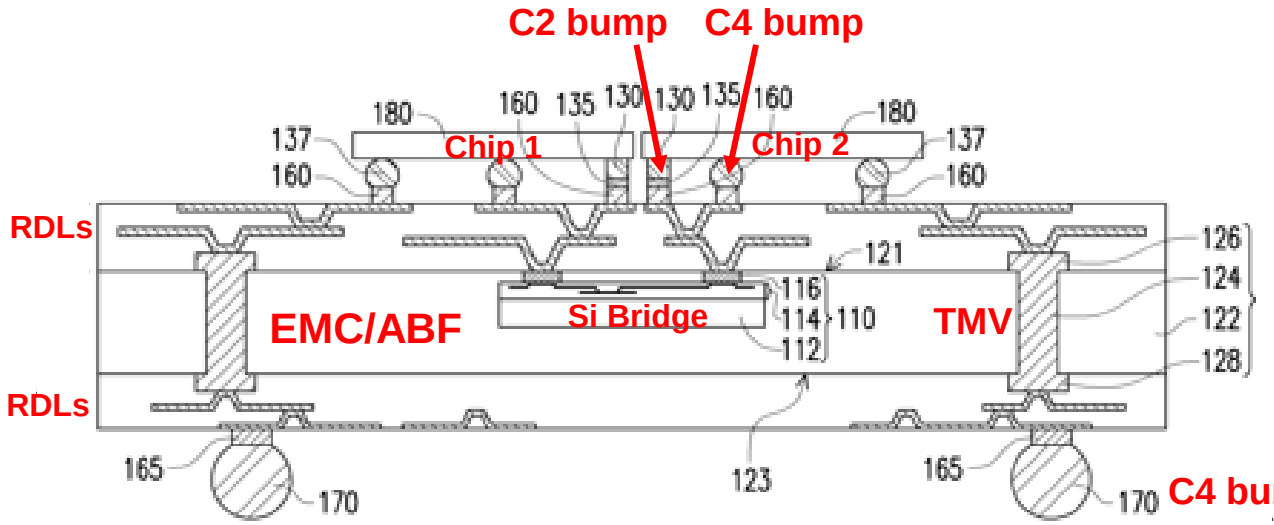
Si bridge on fan-out RDLs



Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC) with Redistribution-Layers (RDLs)

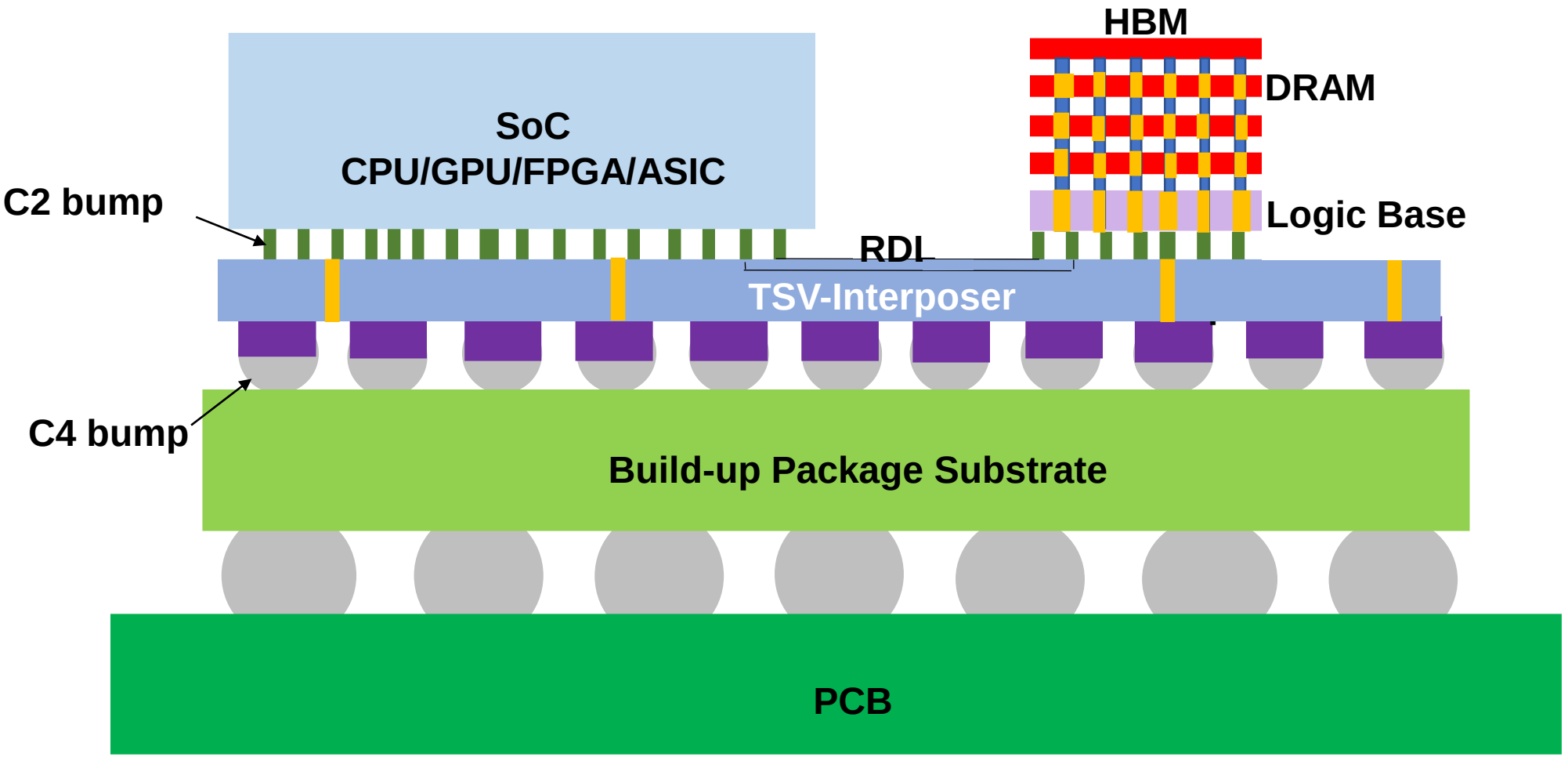
Unimicron's Fan-out Chip (Bridge) First Face-down Process





U.S. patent 11,410,933 (Aug. 9, 2022), filed on May 7, 2021.

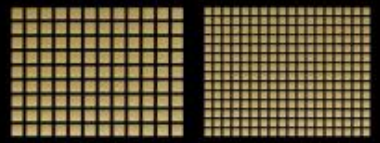
Packaging Technology Driven by Artificial Intelligence (AI)



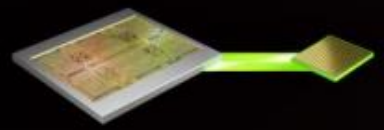
CoWoS (2.5D IC Integration)

NVIDIA A100

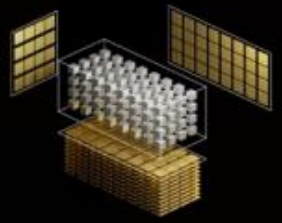
SUPERCHARGING HIGH PERFORMING AI SUPERCOMPUTING GPU



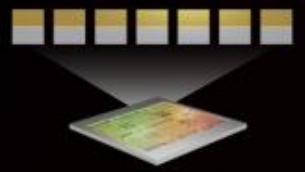
80 GB HBM2e
For largest datasets
and models



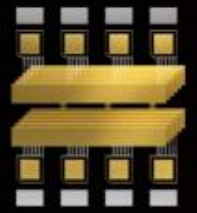
2 TB/s +
High-memory bandwidth
to feed extremely fast GPU



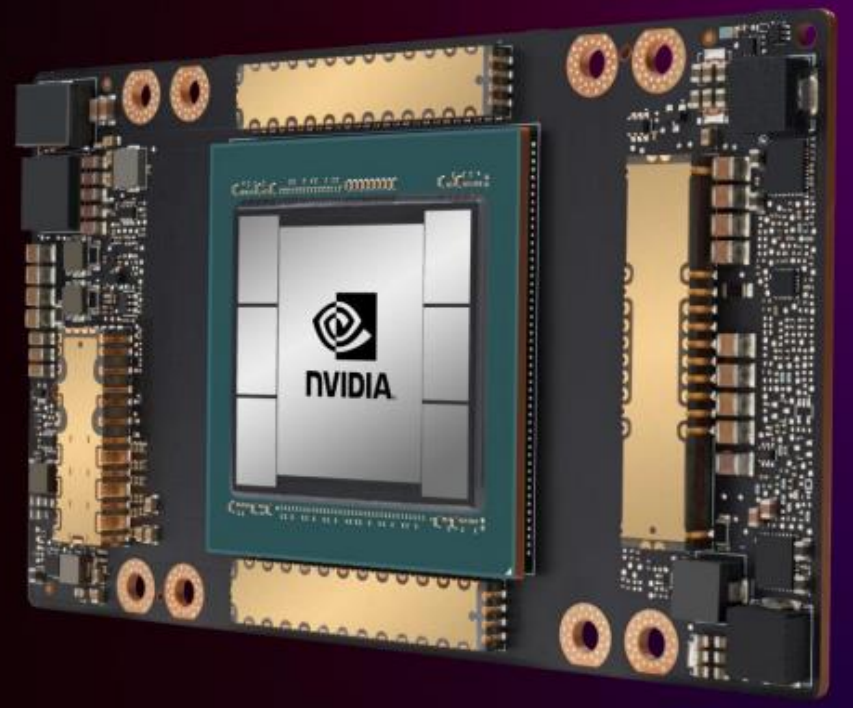
3rd-gen Tensor core



Multi-instance GPU

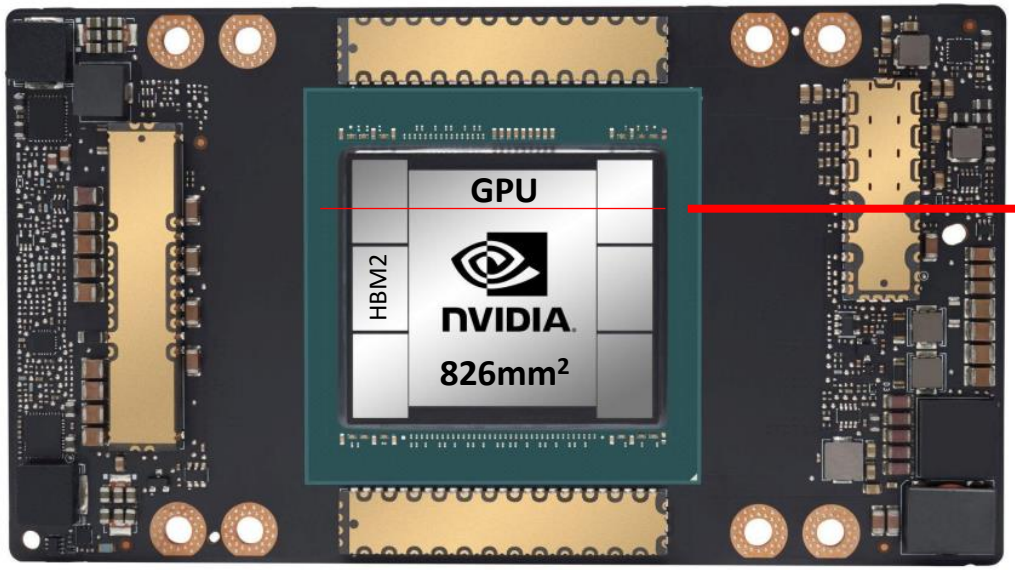


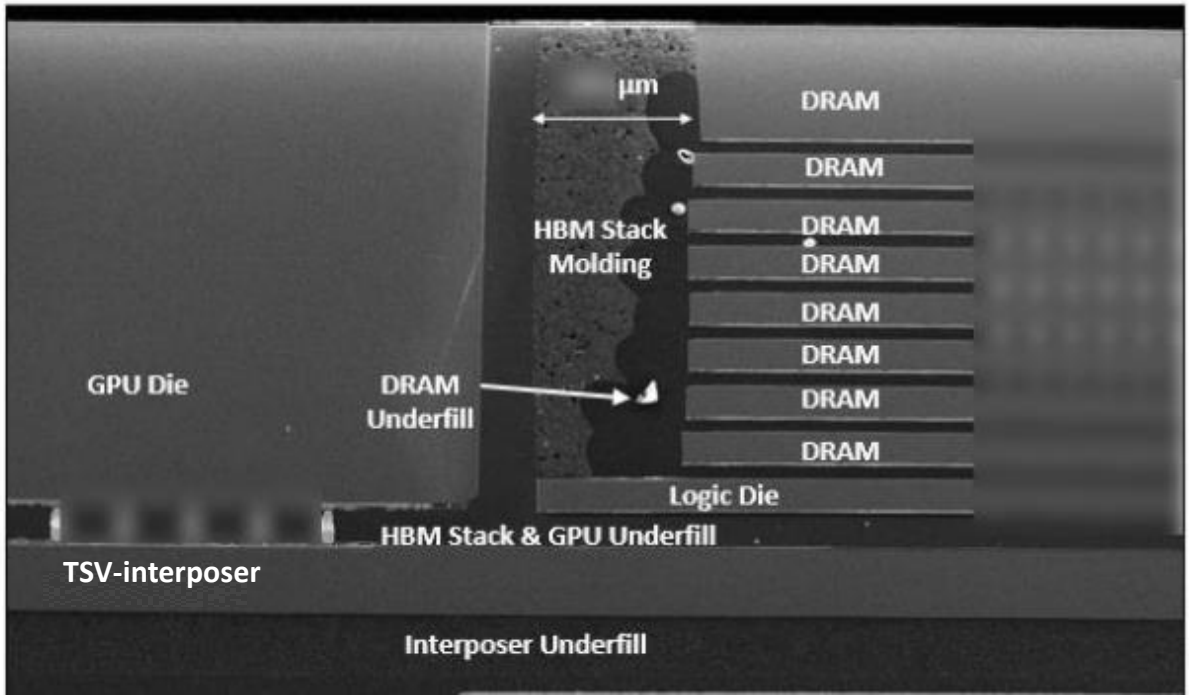
3rd-gen NVLink

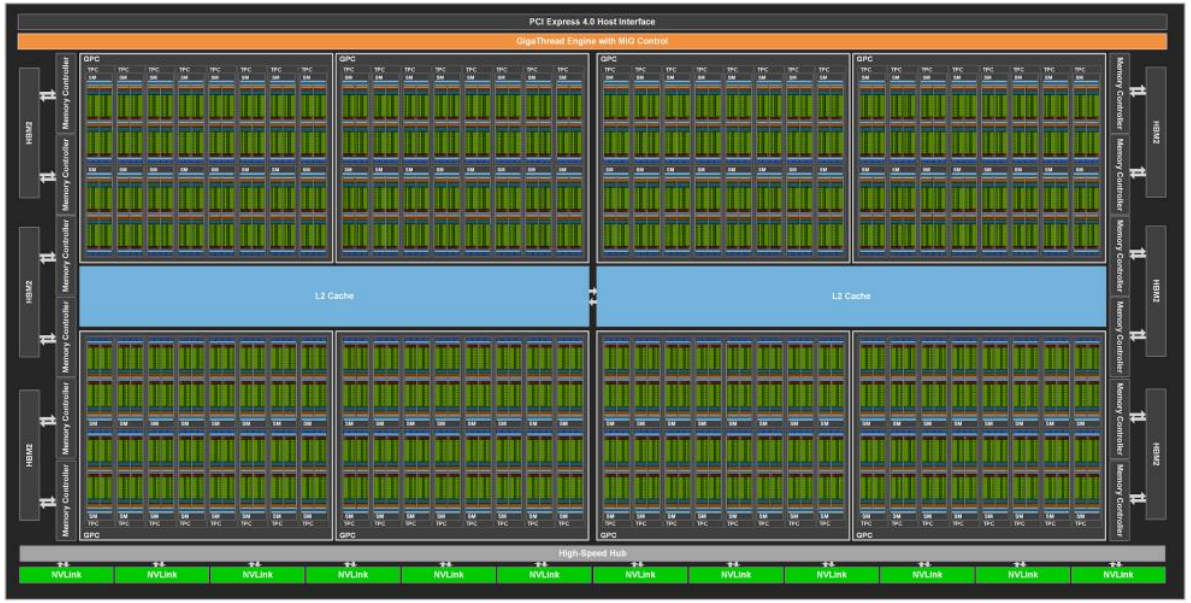


Powering Amazon EC2 P4d/P4de instances

Nvidia's A100 (GPU = 826 mm²) is on a TSV-Interposer

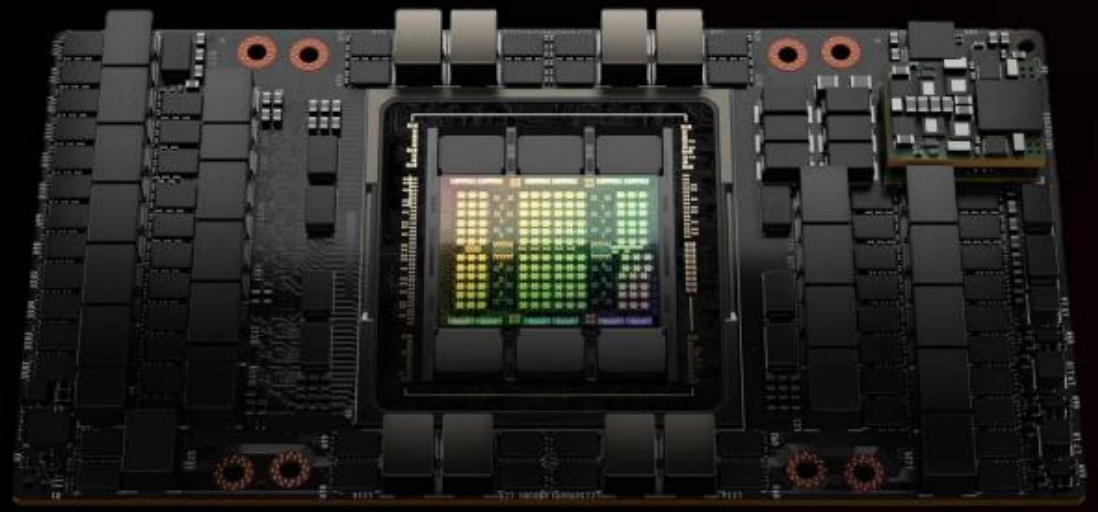




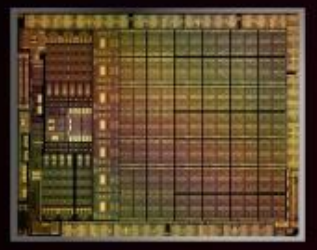


NVIDIA H100 – Coming soon to AWS

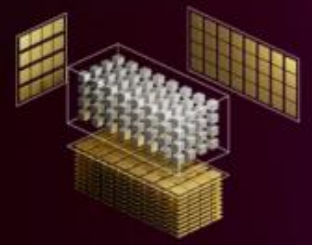
THE NEW ENGINE OF THE WORLD'S AI INFRASTRUCTURE



Powering the next generation of GPU systems on AWS



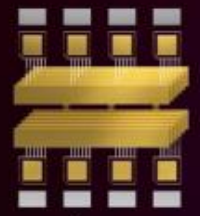
Advanced chip



Transformer engine

2nd-gen MIG

Confidential computing



4th-gen NVLink

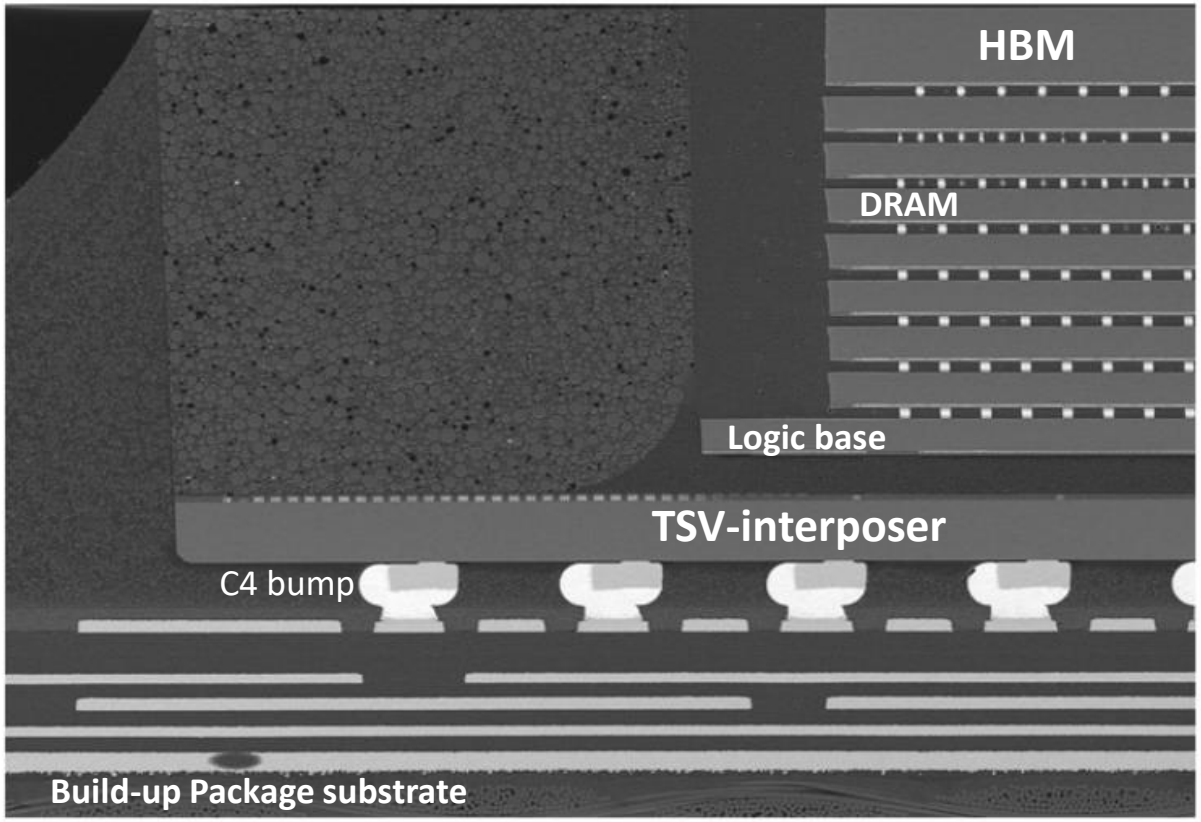
DPX instructions

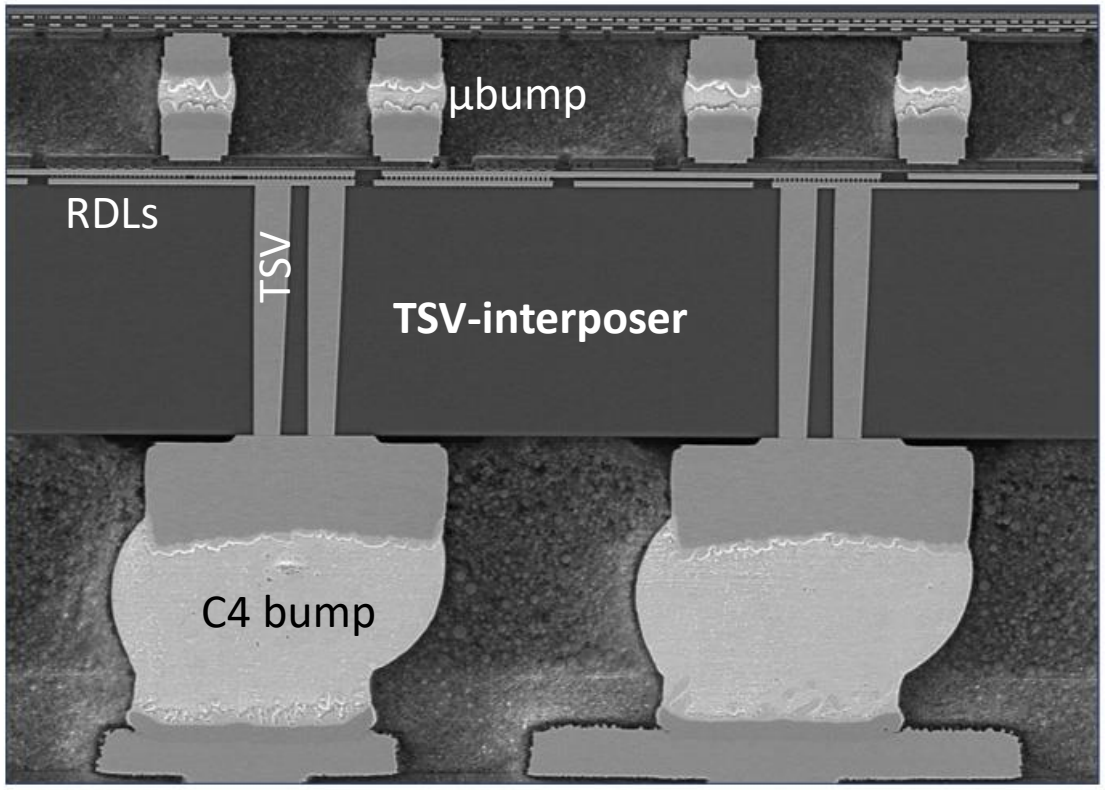
The flagship H100 GPU (14,592 CUDA cores, 80GB of HBM3 capacity, 5,120-bit memory bus) is priced at a massive $30,000 (average), which Nvidia CEO Jensen Huang calls the first chip designed for generative AI.

aws

NVIDIA

NVIDIA H100 GPU for AI Application





CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package

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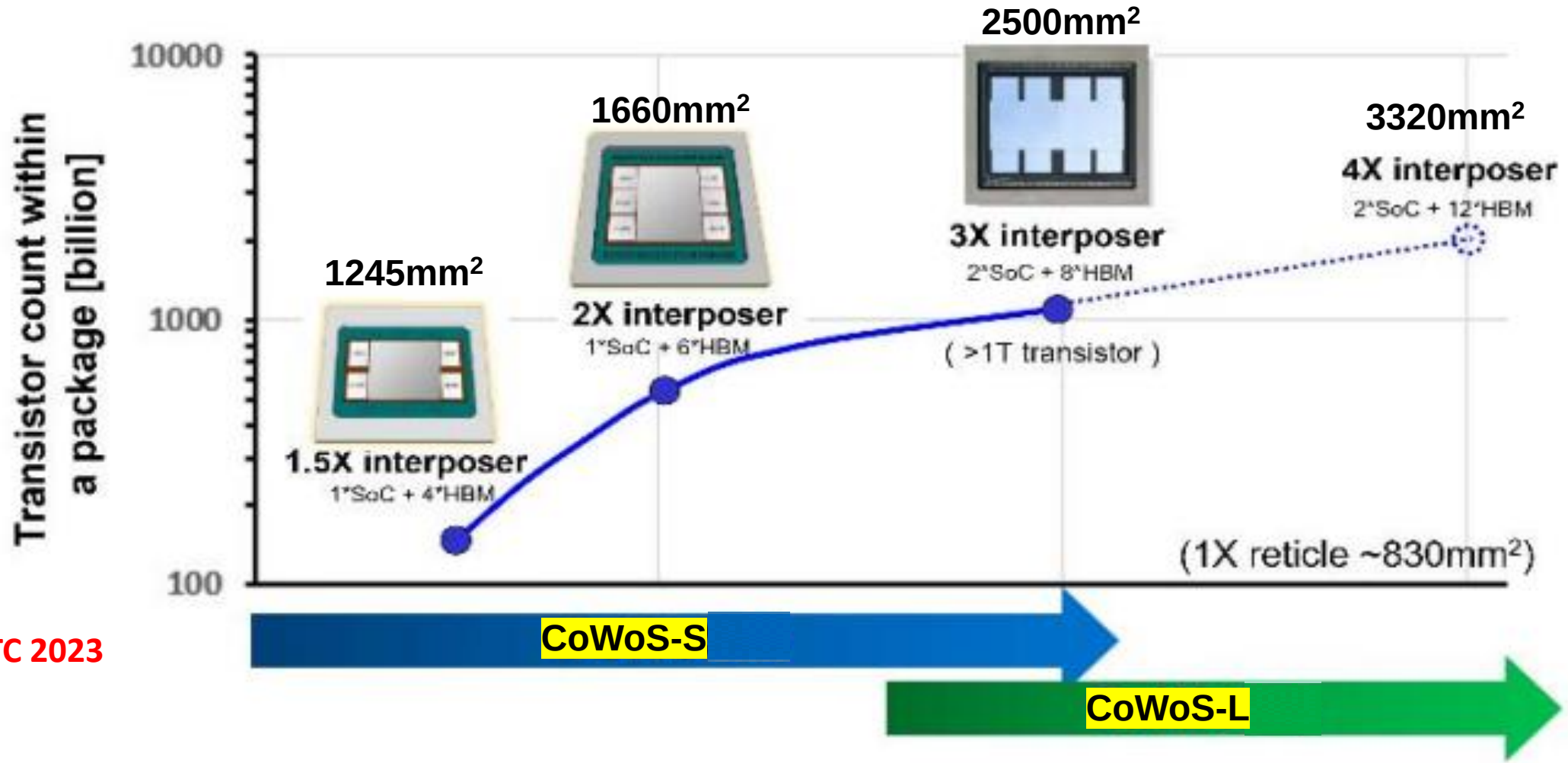
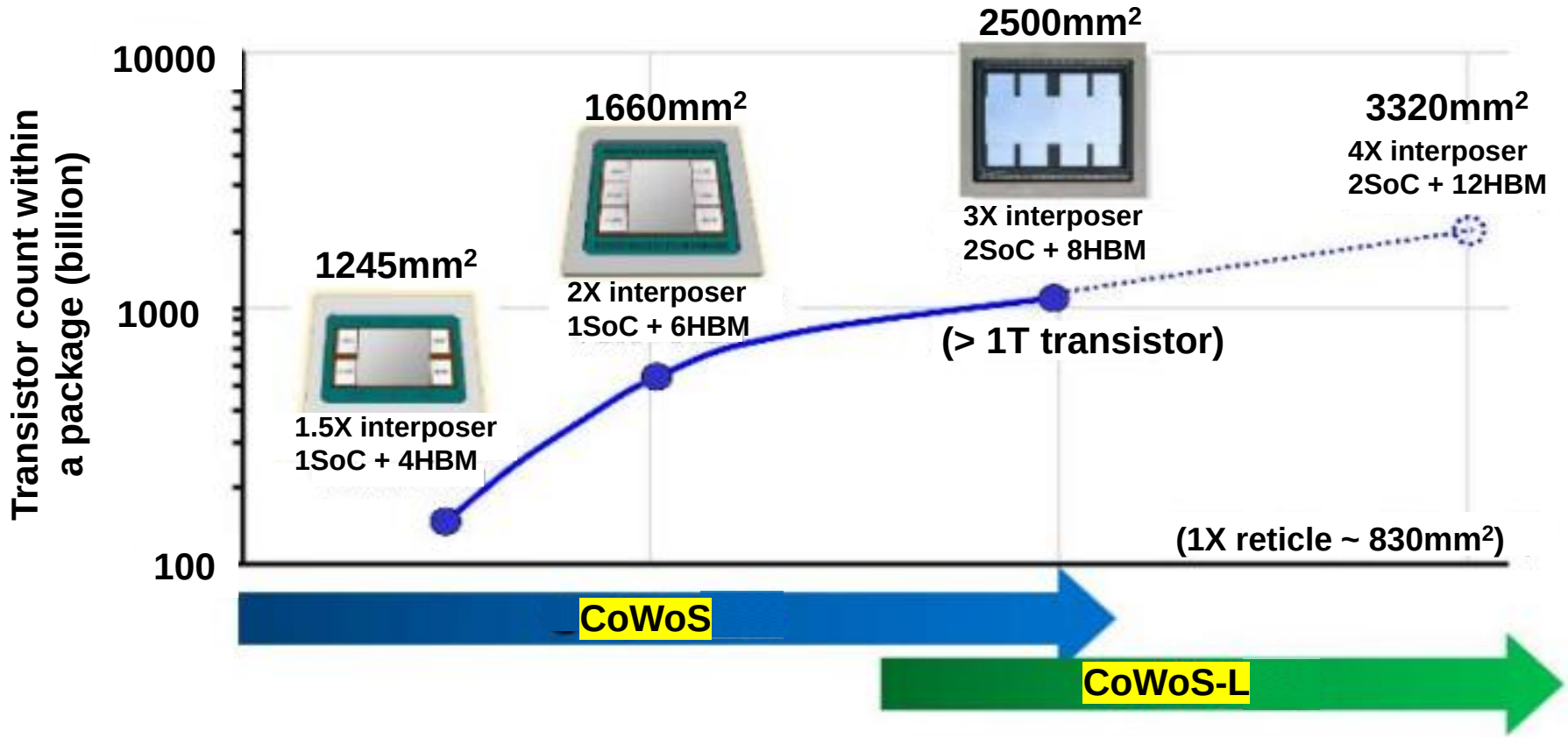
S. Y. Hou

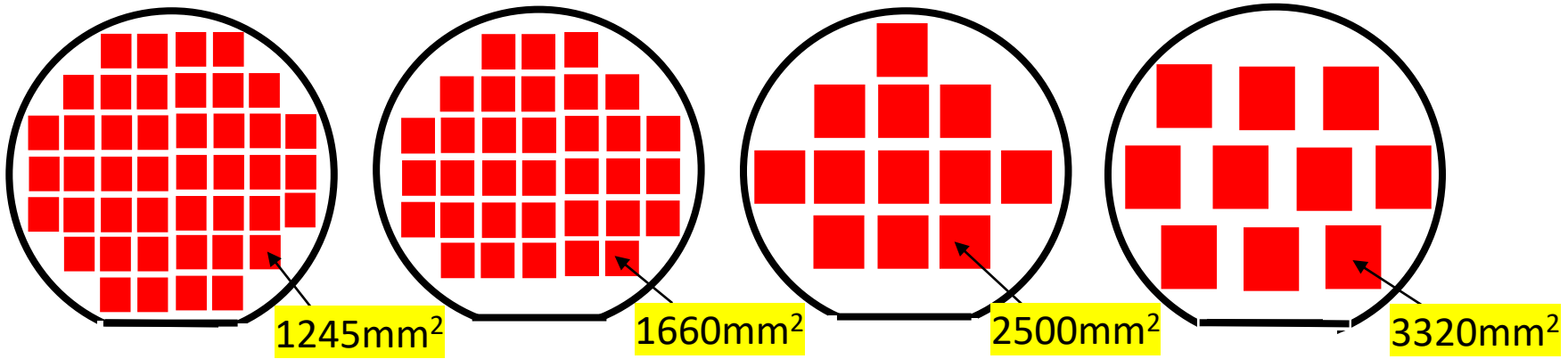


IEEE/ECTC 2023

(a)


Transistor count within a package (billion)
10000
1000
100
1245mm²
1.5X interposer
1SoC + 4HBM
1660mm²
2X interposer
1SoC + 6HBM
2500mm²
3X interposer
2SoC + 8HBM
3320mm²
4X interposer
2SoC + 12HBM
(> 1T transistor)
(1X reticle ~ 830mm²)
CoWoS
CoWoS-L

(b)


1245mm²
1660mm²
2500mm²
3320mm²
44@1245mm²
33@1660mm²
12@2500mm²
10@3320mm²

TSMC CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package

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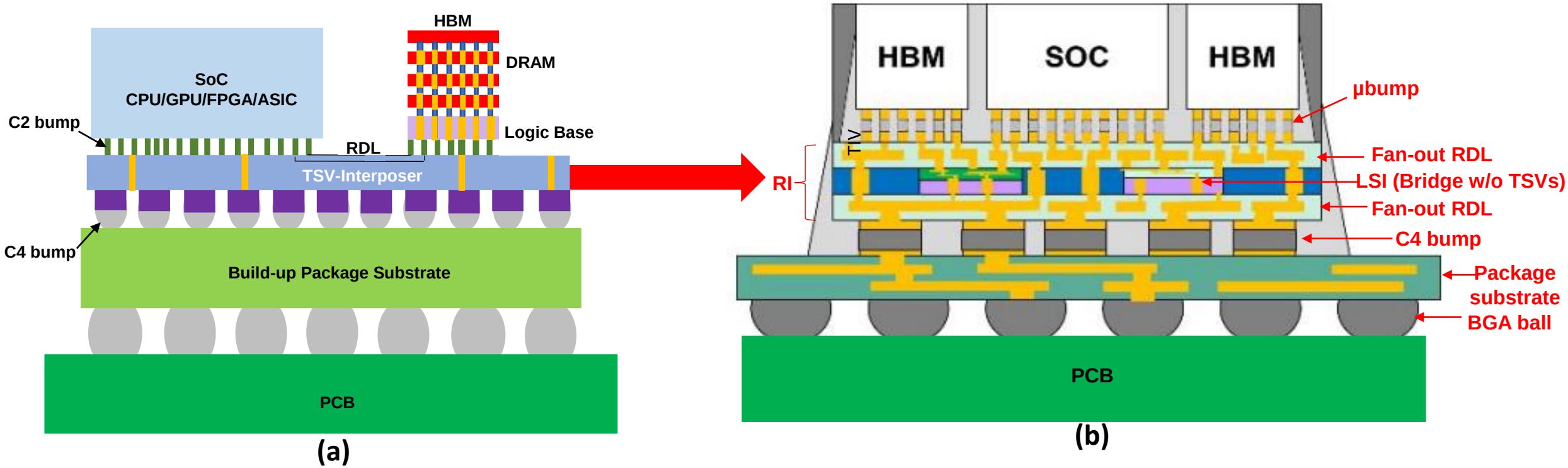


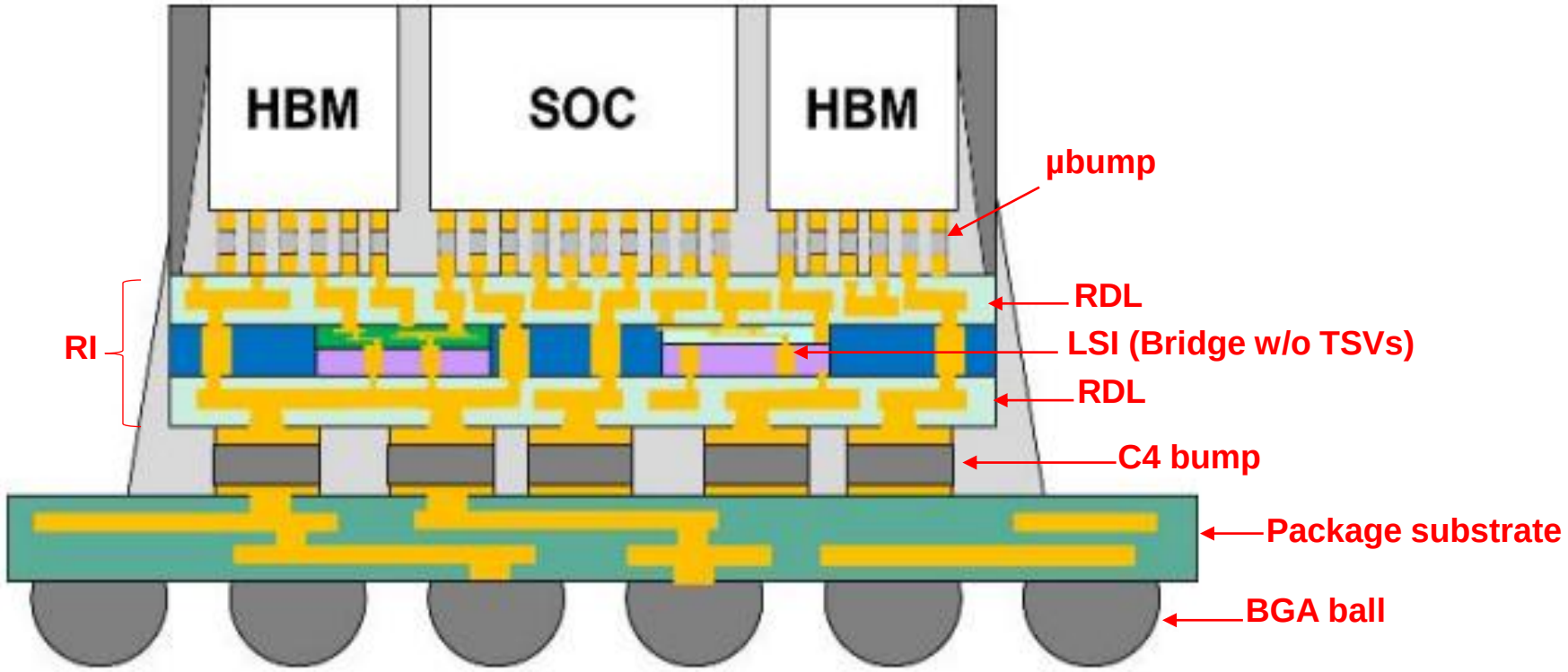
CoWoS (2.5D IC Integration)

CoWoS_L (Bridge with Fan-Out RDLs)

TSV-Interposer is replaced by the RI (Reconstituted-Interposer) which consists of Si Bridge (LSI) embedded in EMC with fan-out RDLs

TSMC's CoWoS_L
LSI (Locsl Silicon Interconnect) + Organic Interposer

ECTC2023



CoWoS-L

- The new interposer which consists of multiple local Si interconnect (LSI or bridge) w/o TSV and global integrated fan-out (InFO) redistribution layers (RDL) to form a reconstituted interposer (RI).
- The small-size LSI (bridge) inherits all the attractive features of TSV-interposer by retaining sub-micron Cu interconnects, through silicon vias (TSV), and embedded deep trench capacitor (eDTC) to ensure good system performance, while avoids the issues associated with one large TSV-interposer, such as yield loss.

Fan-Out Embedded Bridge with TSV (FO-EB-T) Package Characterization and Evaluation

ECTC2023

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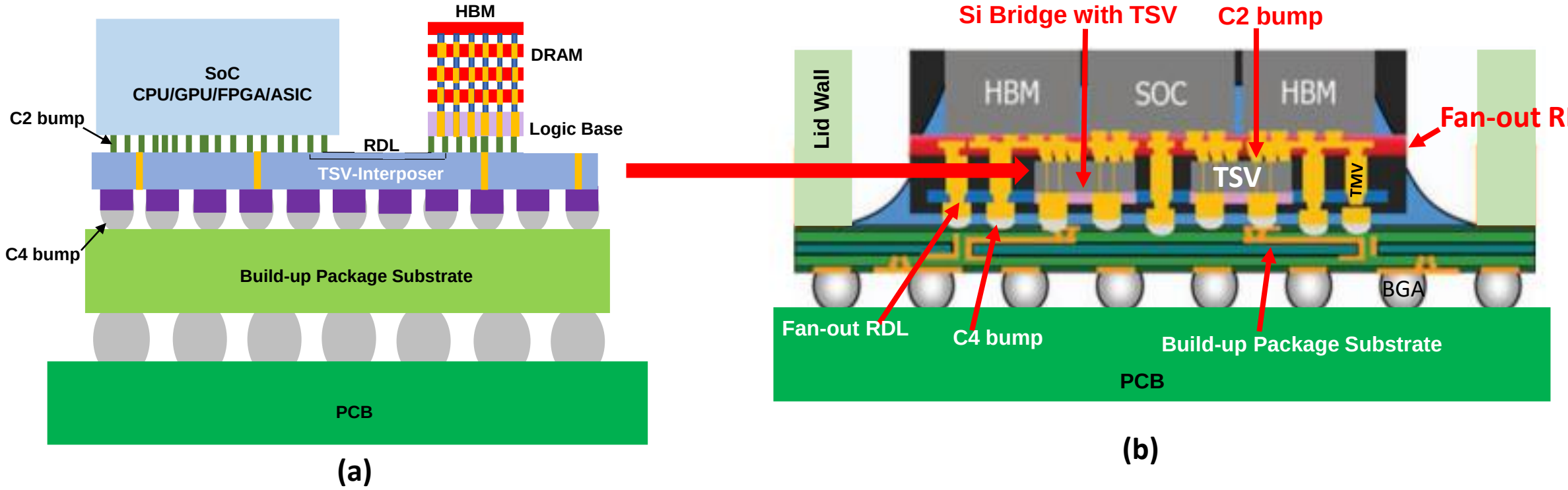
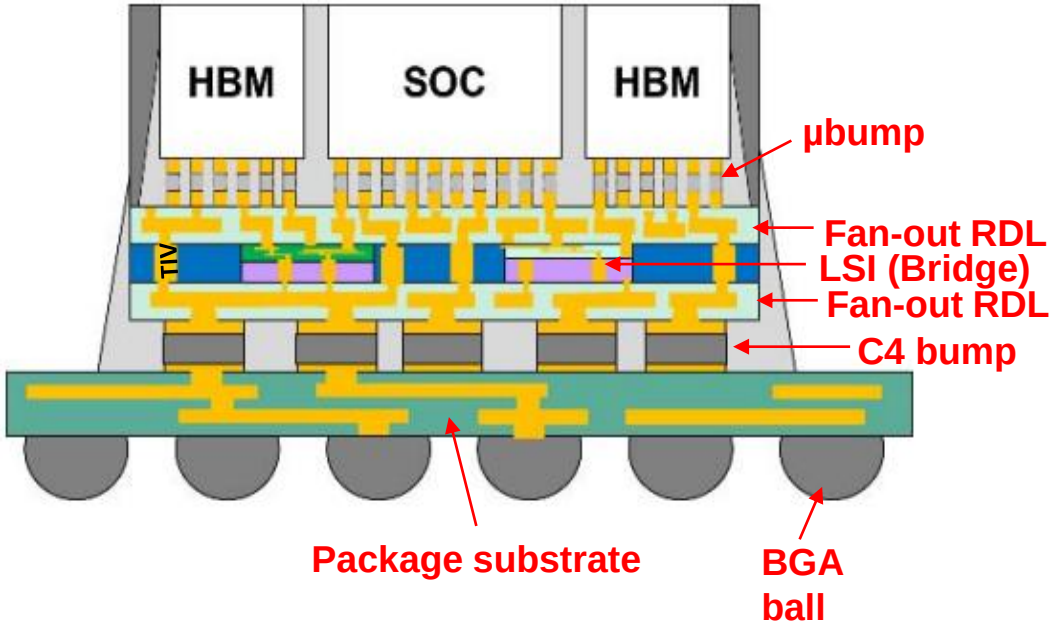


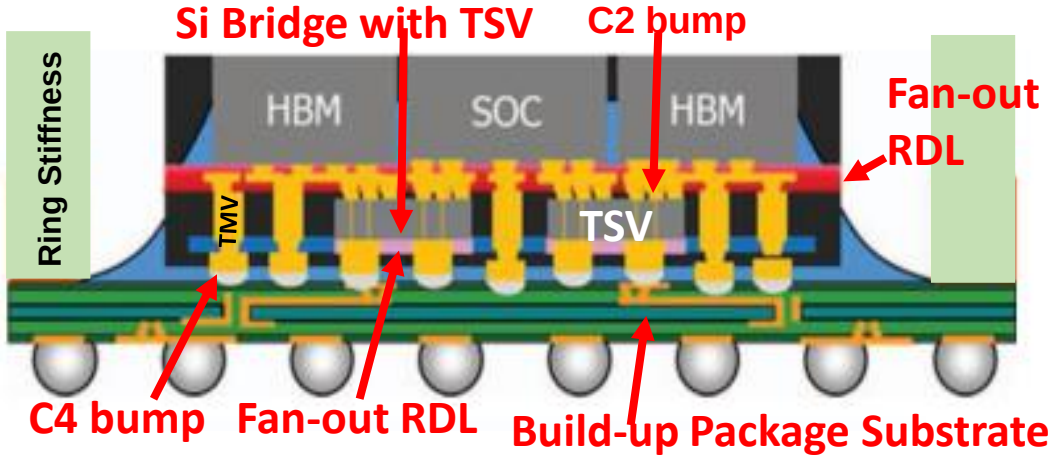
TSV-Interposer is replaced by the FO-EB-T, which consists of Si Bridge with TSVs embedded in the EMC with fan-out RDLs

Similarity between CoWoS-L/FO-EB-T and US 11,410,933

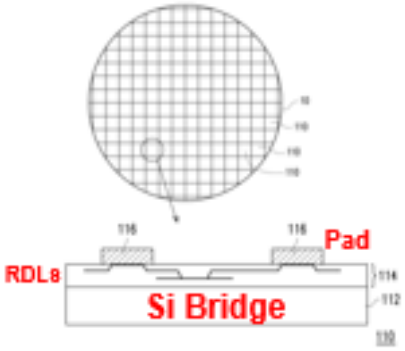
TSMC's CoWoS_L

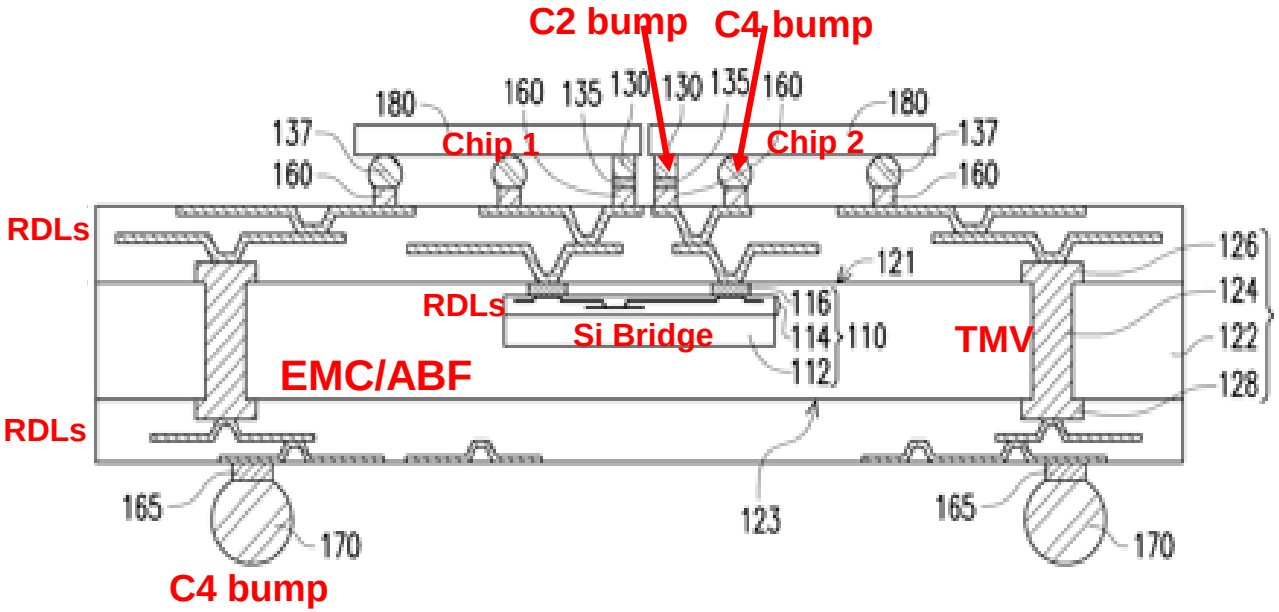


SPIL's FO-EB-T



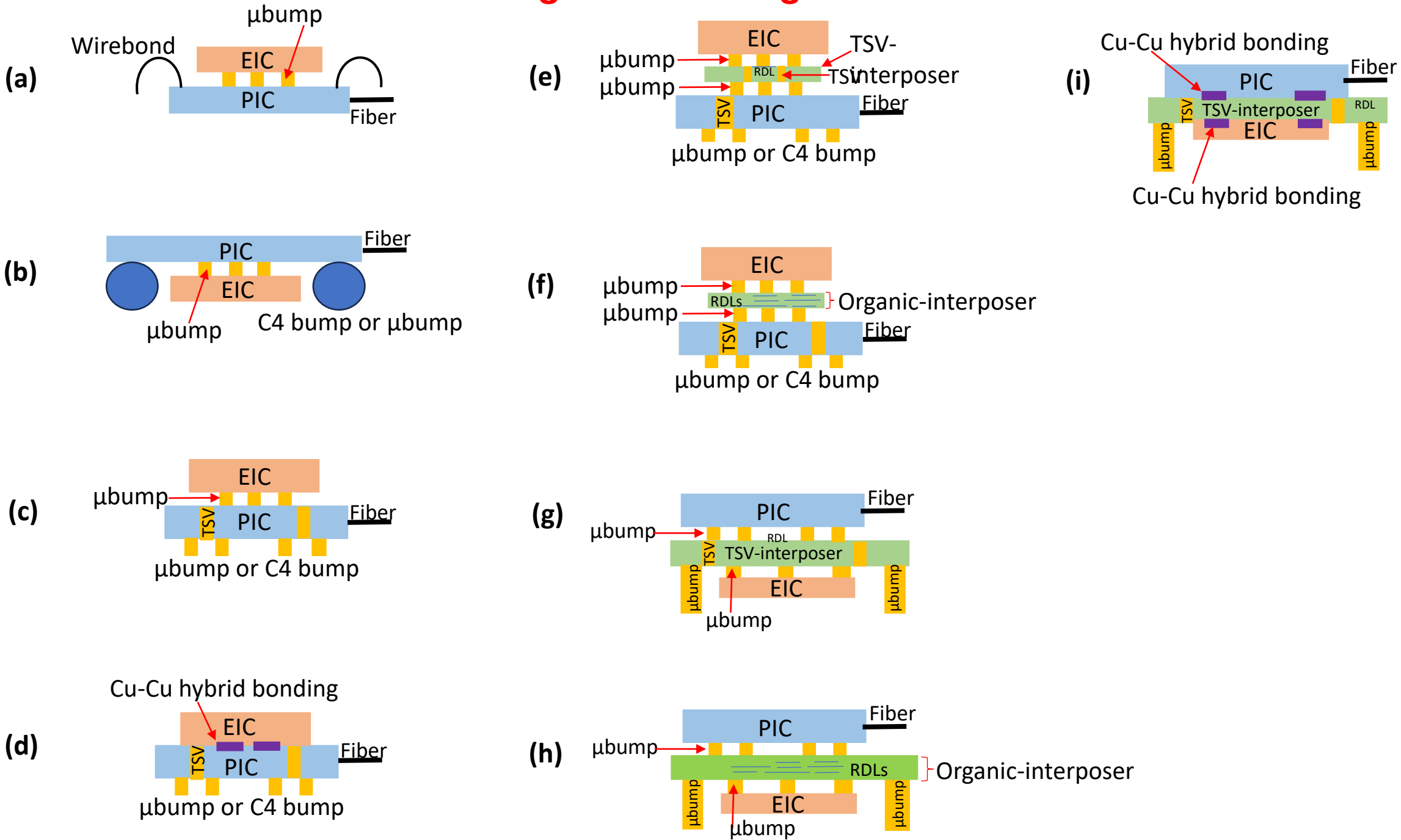
Bridge Patent: US 11,410,933



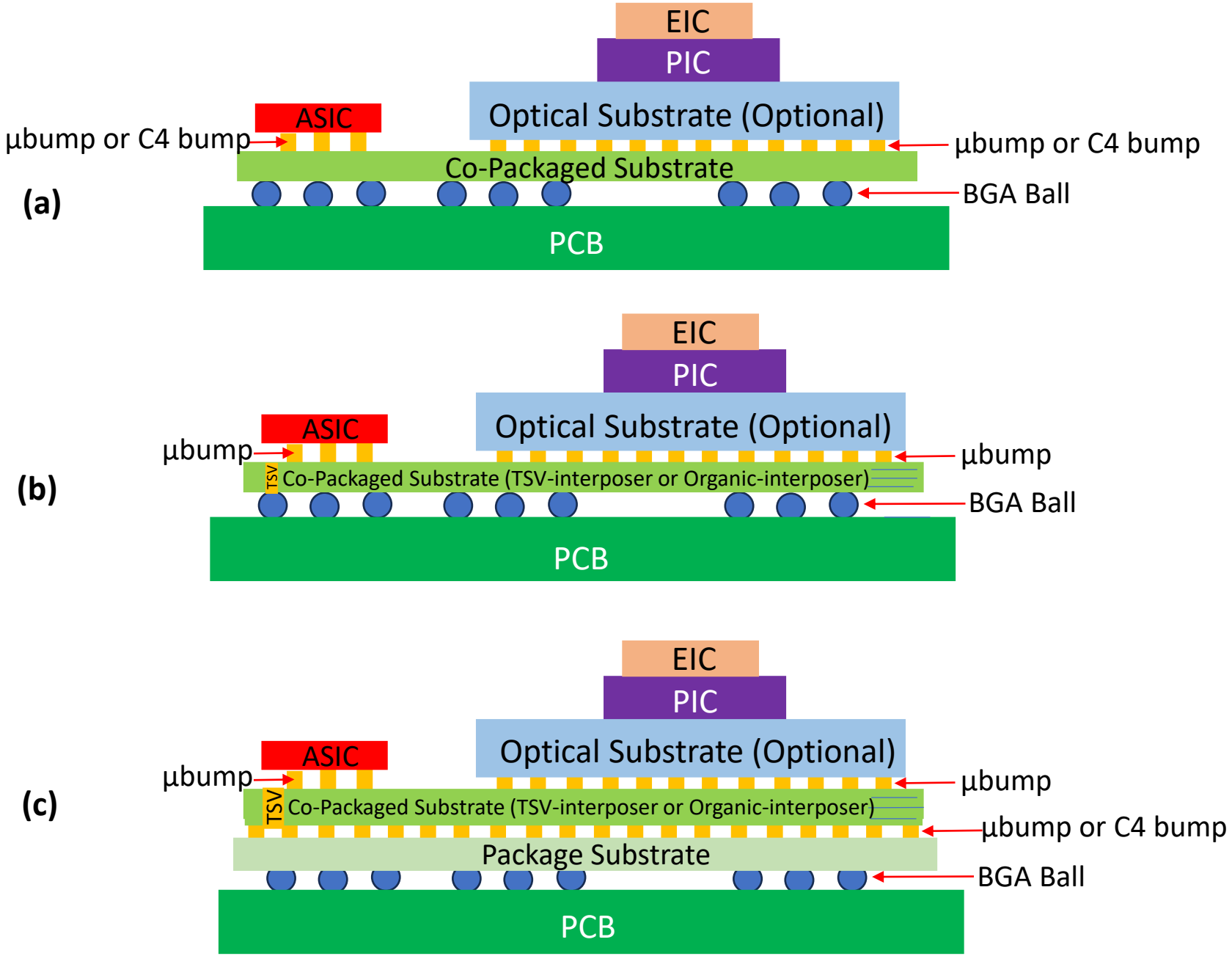


US 11,410,933, Aug. 9, 2022, Filed on May 7, 2021

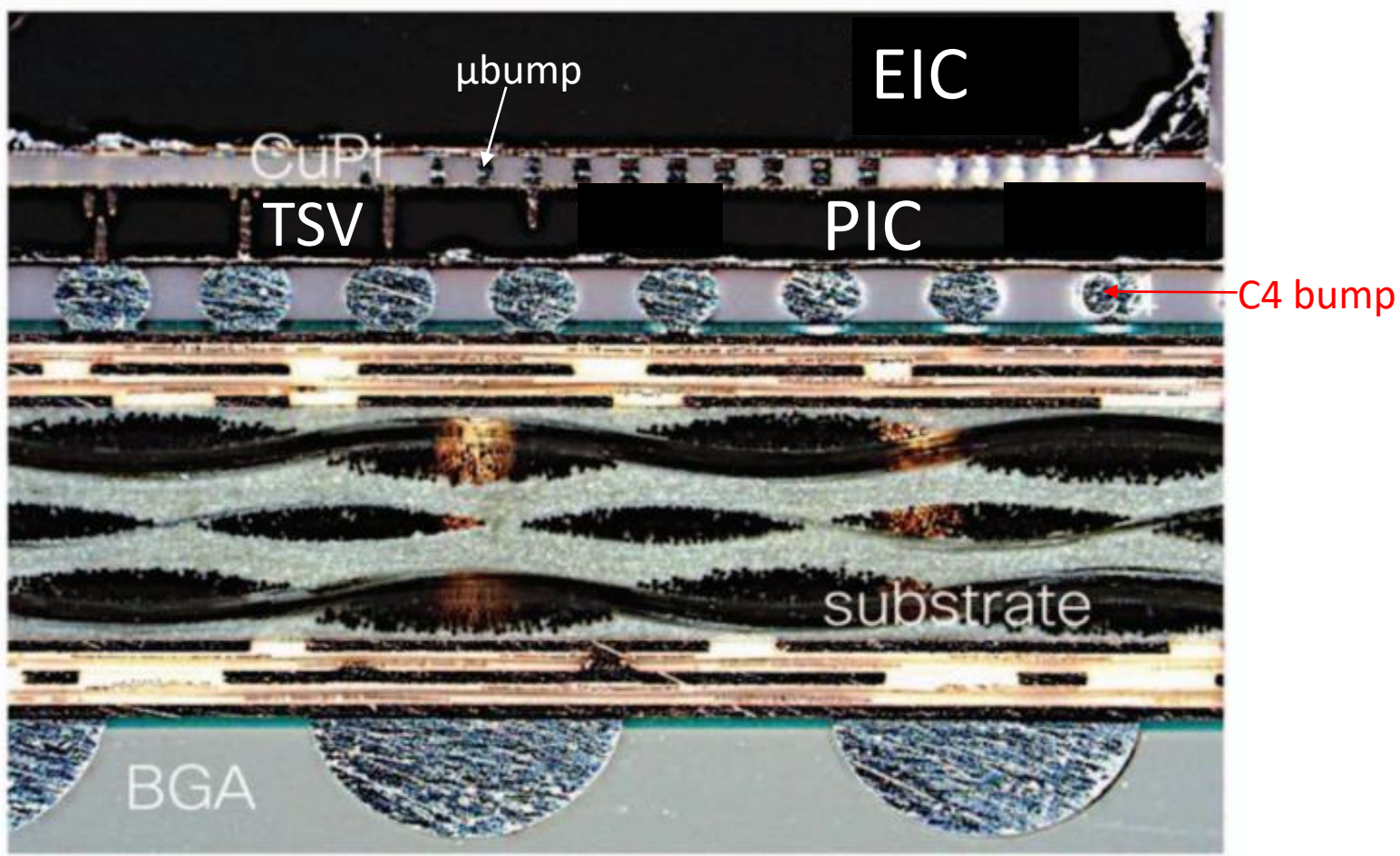
Various 3D heterogeneous integration of EIC and PIC



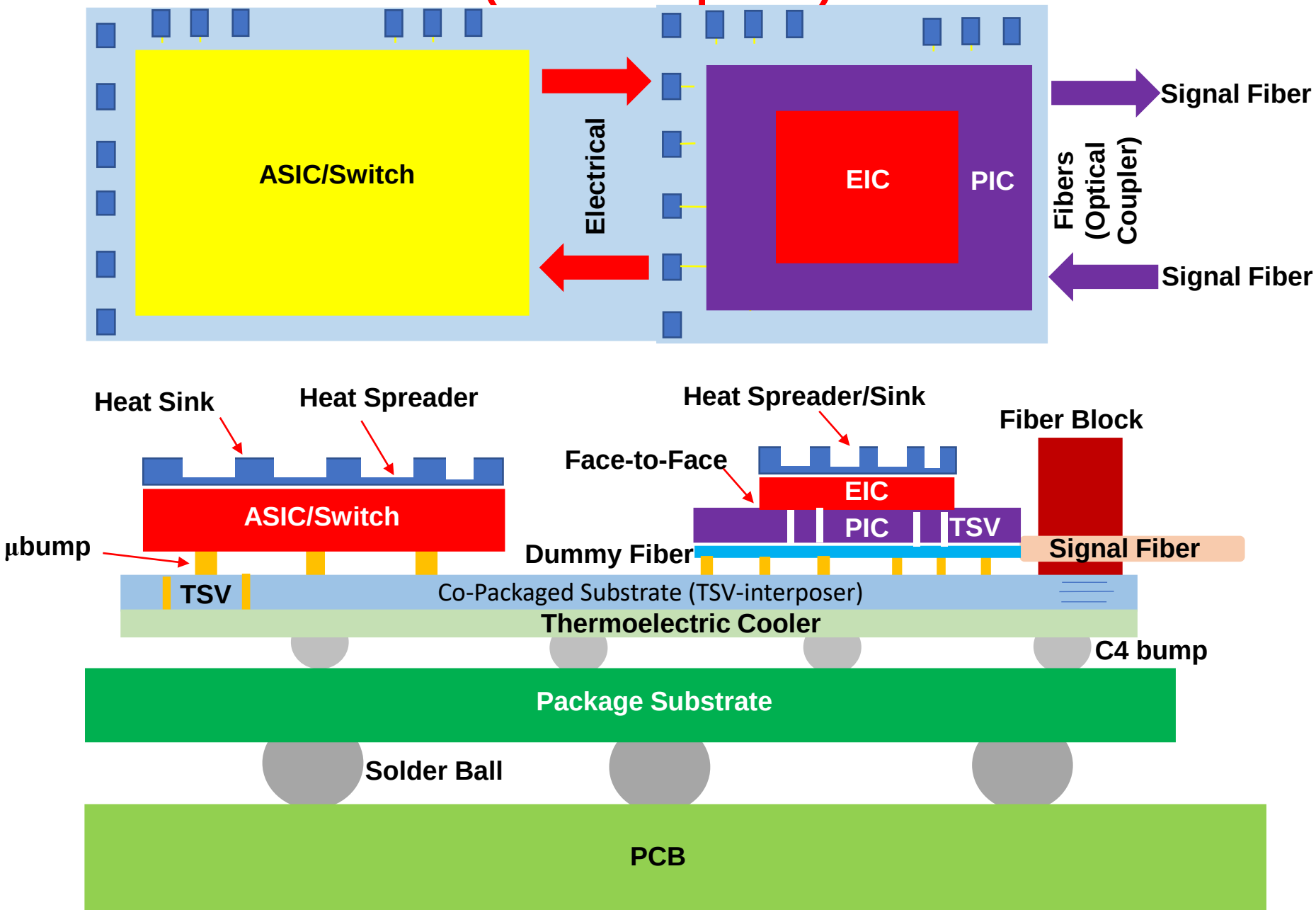
3D heterogeneous integration of ASIC, EIC and PIC. (a) On an ordinary co-packaged substrate. (b) On TSV-interposer or organicinterposer. (c) On TSV-interposer or organicinterposer and then on package substrate.



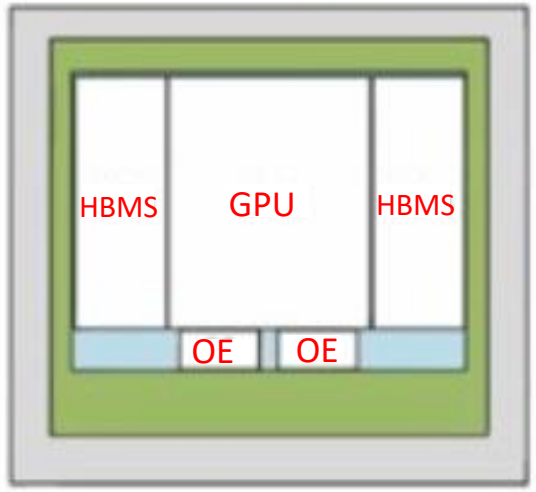
3D heterogeneous integration of EIC and PIC on a co-packaged substrate (organic interposer)



3D heterogeneous integration of ASIC, EIC and PIC on a co-packaged substrate (TSV interposer)

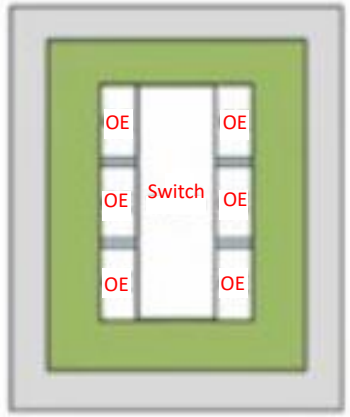


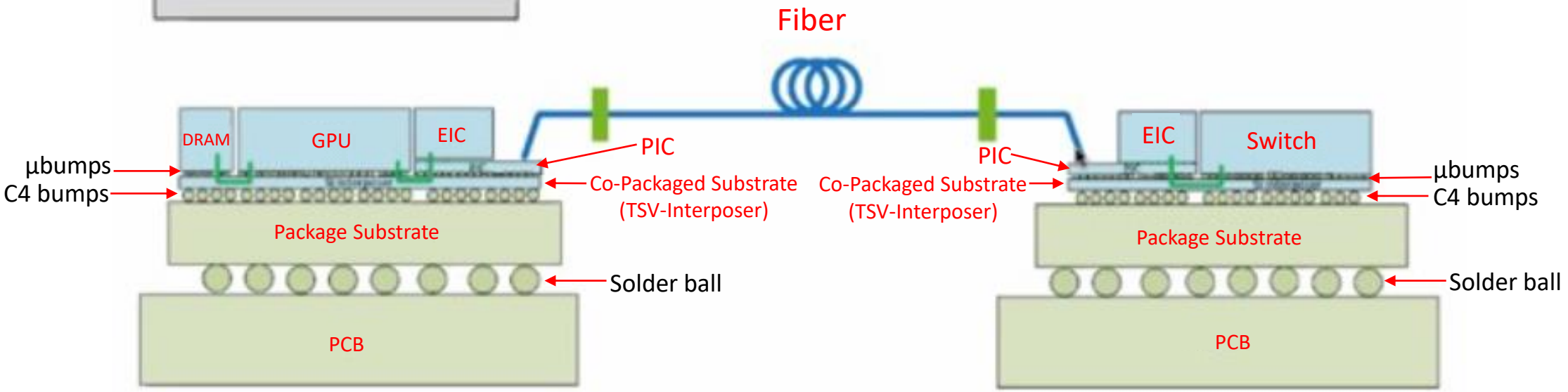
Nvidia's 3D integration of SoC, HBM, EIC and PIC on co-packaged substrates (TSV interposer)



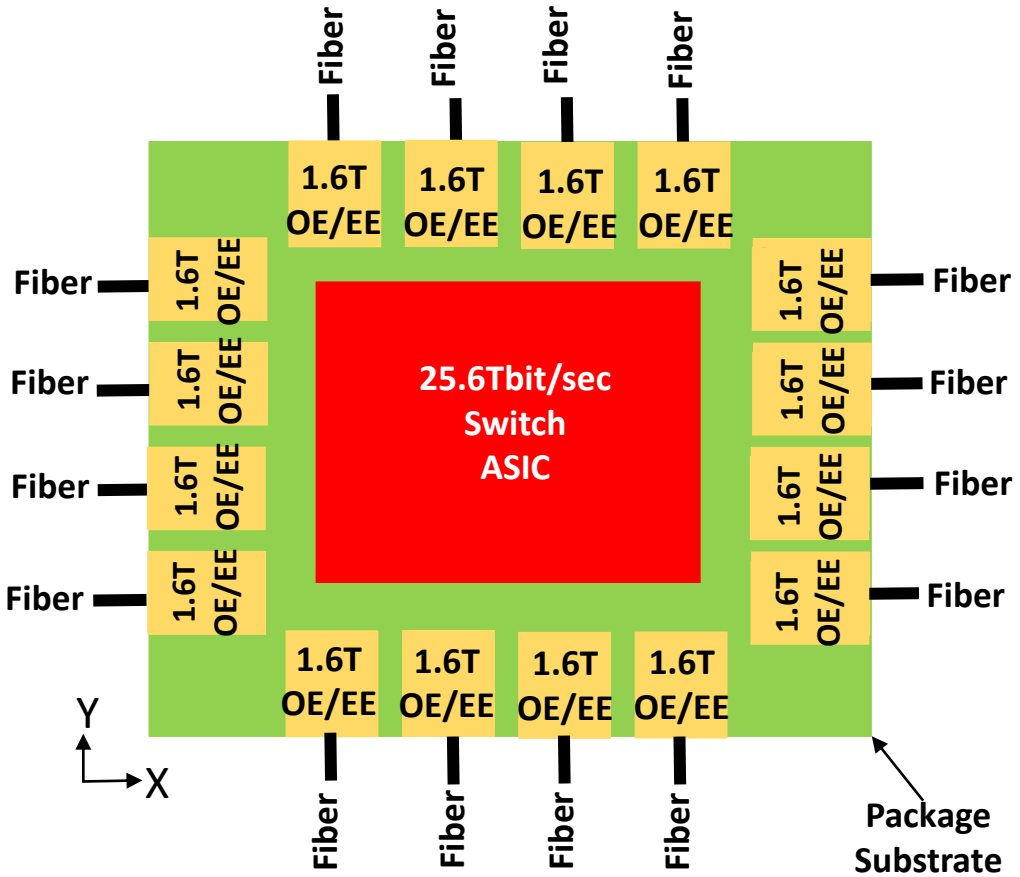
Optical Engine (OE)

- 24 NYLINKs
- 4.8Tbps per direction
- 24 laser fibers
- 24 Tx fibers
- 24 Rx fibers
- 5mm x 10mm

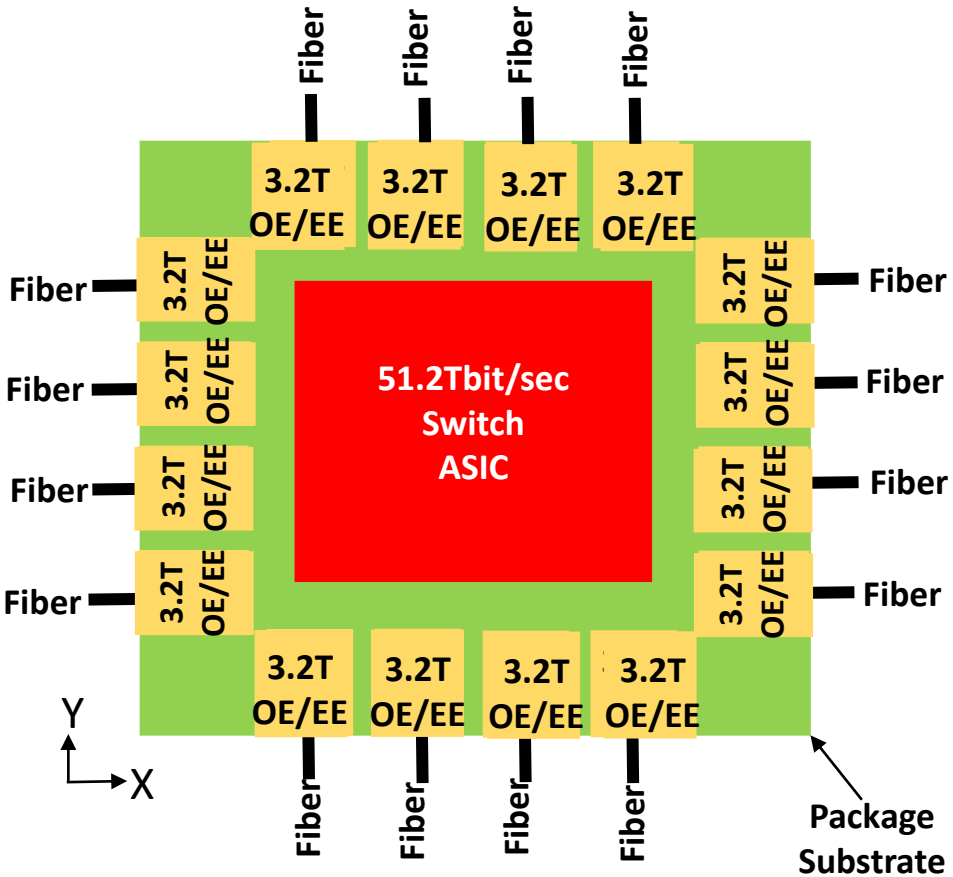




The present switch (25.6Tbit/s) vs. the future switch (51.2Tbit/s)

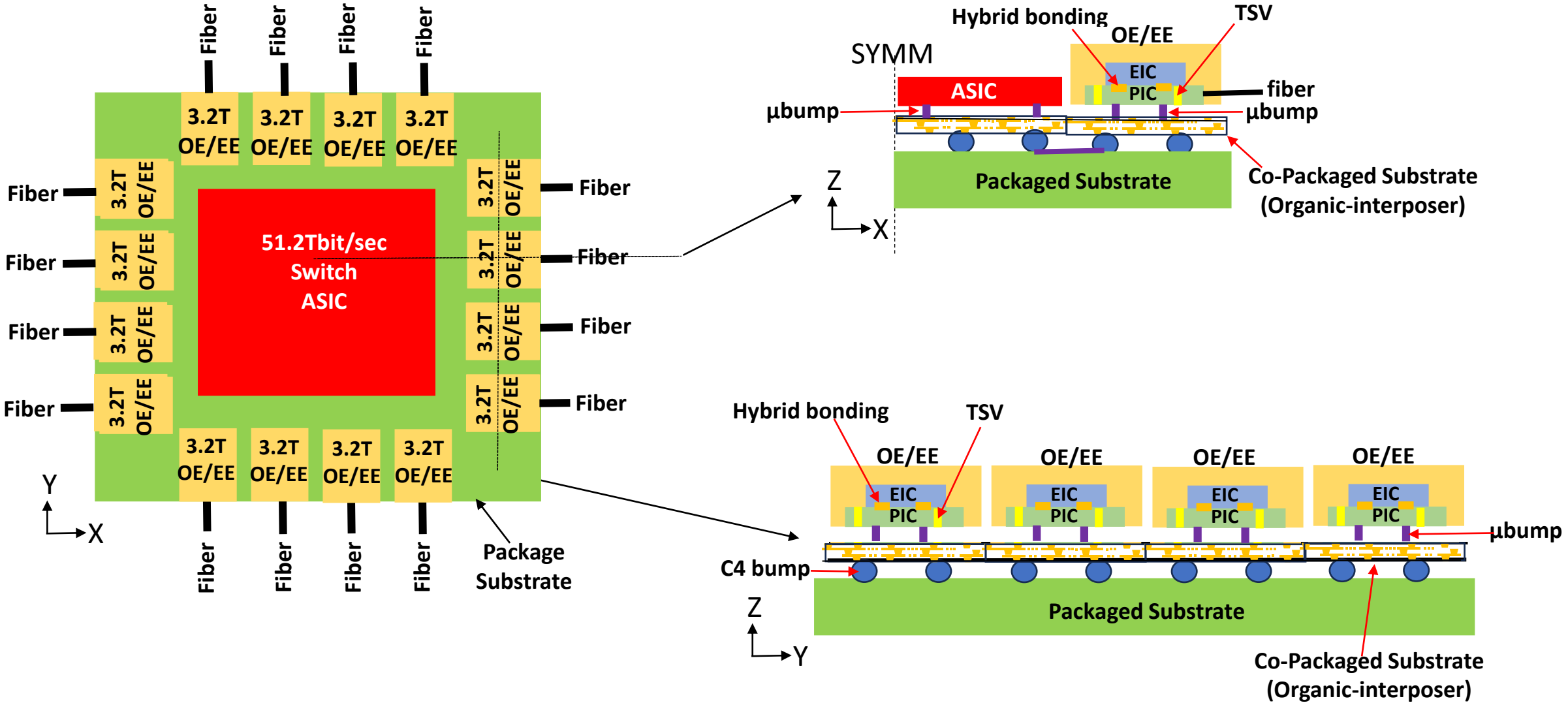


Present

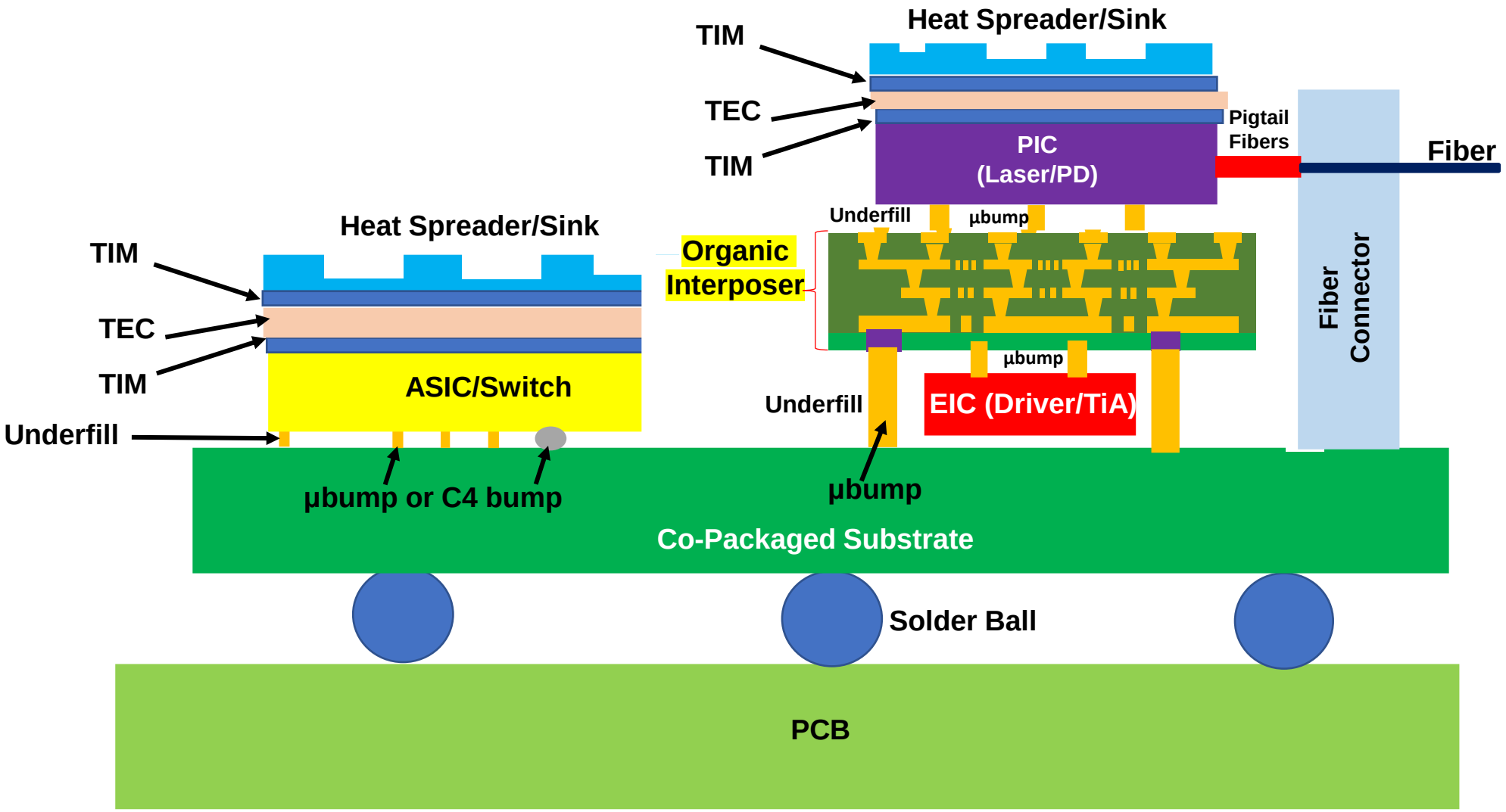


Future

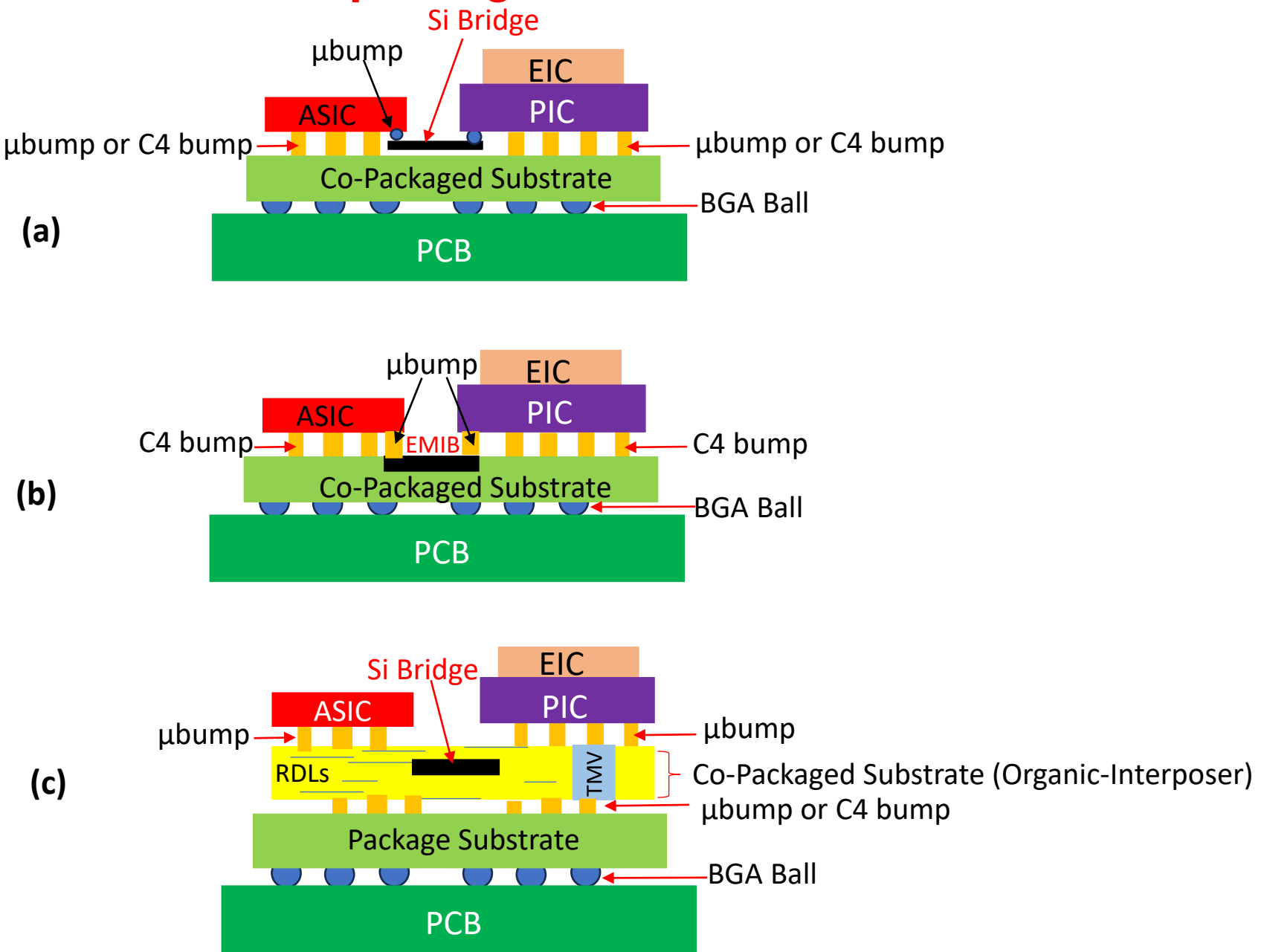
3D Heterogeneous Integration of EIC and PIC (B)



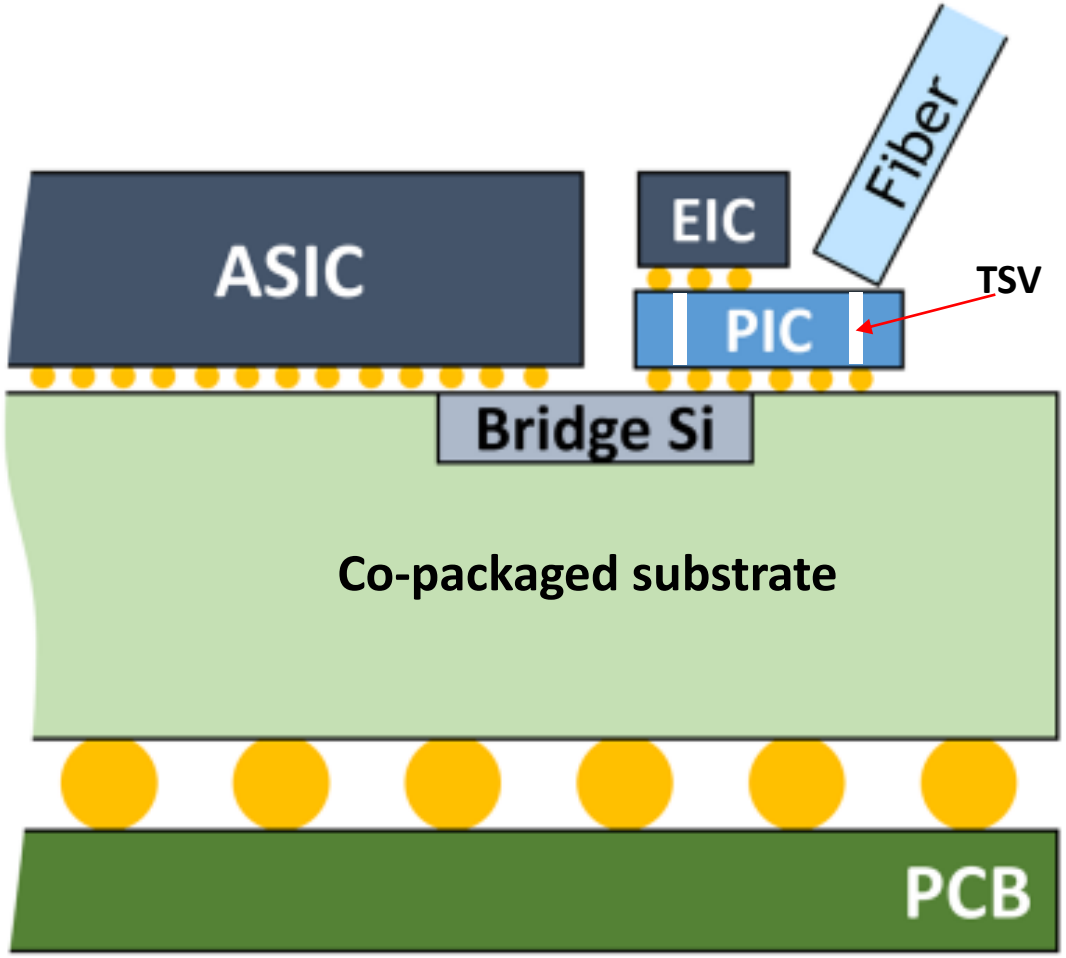
Another Co-packaged optics method for 51.2Tbit/s switch



3D heterogeneous integration of ASIC, EIC and PIC with silicon bridges on a co-packaged substrate



An example on 3D heterogeneous integration of ASIC, EIC and PIC with silicon bridges on a co-packaged substrate



On September 18, 2023, …

Intel has announced a new glass-substrate technology for the next generation of high-power processors.

Intel is on the path to delivering 1 trillion transistors on a package by 2030 and its ongoing innovation in advanced packaging including glass substrates will help achieve this goal.

Intel Unveils Industry-Leading Glass Substrates to Meet Demand for More Powerful Compute

Glass substrates help overcome limitations of organic materials by enabling an order of magnitude improvement in design rules needed for future data centers and AI products.

Intel PR, September 18, 2023

What's New: Intel today announced one of the industry's first glass substrates for next-generation advanced packaging, planned for the latter part of this decade. This breakthrough achievement will enable the continued scaling of transistors in a package and advance Moore's Law to deliver data-centric applications.

"After a decade of research, Intel has achieved industry-leading glass substrates for advanced packaging. We look forward to delivering these cutting-edge technologies that will benefit our key players and foundry customers for decades to come."

–Babak Sabi, Intel senior vice president and general manager of Assembly and Test Development

Why It Matters: Compared to today's organic substrates, glass offers distinctive properties such as ultra-low flatness and better thermal and mechanical stability, resulting in much higher interconnect density in a substrate. These benefits will allow chip architects to create high-density, high-performance chip packages for data-intensive workloads such as artificial intelligence (AI). Intel is on track to deliver complete glass substrate solutions to the market in the second half of this decade, allowing the industry to continue advancing Moore's Law beyond 2030.

By the end of the decade, the semiconductor industry will likely reach its limits on being able to scale transistors on a silicon package using organic materials, which use more power and include limitations like shrinkage and warping. Scaling is crucial to the progress and evolution of the semiconductor industry, and glass substrates are a viable and essential next step for the next generation of semiconductors.

How It Works: As the demand for more powerful computing increases and the semiconductor industry moves into the heterogeneous era that uses multiple "chiplets" in a package, improvements in signaling speed, power delivery, design rules and stability of package substrates will be essential. Glass substrates possess superior mechanical, physical and optical properties that allow for more transistors to be connected in a package, providing better scaling and enabling assembly of larger chiplet complexes (called "system-in-package") compared to organic substrates in use today. Chip architects will have the ability to pack more tiles – also called chiplets – in a smaller footprint on one package, while achieving performance and density gains with greater flexibility and lower overall cost and power usage.

About the Use Cases: Glass substrates will initially be introduced into the market where they can be leveraged the most: applications and workloads requiring larger form factor packages (i.e., data centers, AI, graphics) and higher speed capabilities.

Glass substrates can tolerate higher temperatures, offer 50% less pattern distortion, and have ultra-low flatness for improved depth of focus for lithography, and have the dimensional stability needed for extremely tight layer-to-layer interconnect overlay. As a result of these distinctive properties, a 10x increase in interconnect density is possible on glass substrates. Further, improved mechanical properties of glass enable ultra-large form-factor packages with very high assembly yields.

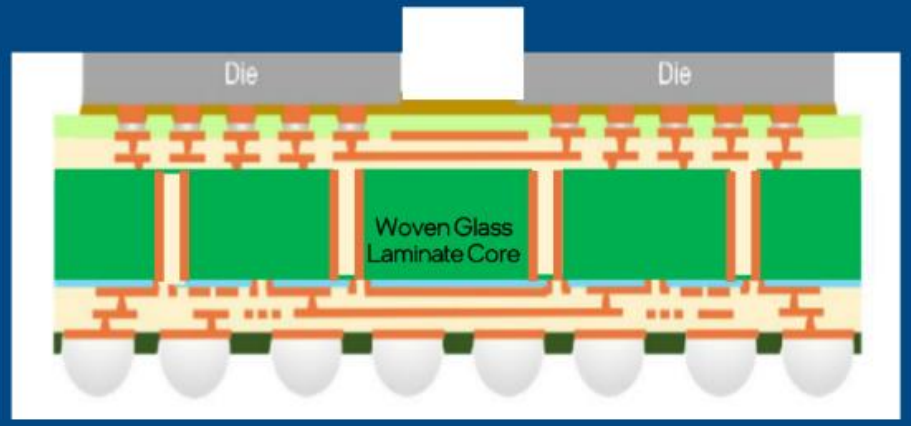
Glass substrates' tolerance to higher temperatures also offers chip architects flexibility on how to set the design rules for power delivery and signal routing because it gives them the ability to seamlessly integrate optical interconnects, as well as embed inductors and capacitors into the glass at higher temperature processing. This allows for better power delivery solutions while achieving high-speed signaling that is needed at much lower power. These many benefits bring the industry closer to being able to scale 1 trillion transistors on a package by 2030.

How We Do It: Intel has been researching and evaluating the reliability of glass substrates as a replacement for organic substrates for more than a decade. The company has a long history of enabling next-generation packaging, having led the industry in the transition from ceramic package to organic package in the 1990s, being the first to enable halogen and lead-free packages, and being the inventor of advanced embedded die packaging technologies, the industry's first active 3D stacking technologies. As a result, Intel has been able to unlock an entire ecosystem around these technologies from equipment, chemical and materials suppliers to substrate manufacturers.

What's Next: Building on the momentum of recent PowerVia and RibbonFET breakthroughs, these industry-leading glass substrates for advanced packaging demonstrate Intel's forward focus and vision for the next era of compute beyond the Intel 18A process node. Intel is on the path to delivering 1 trillion transistors on a package by 2030 and its ongoing innovation in advanced packaging including glass substrates will help achieve this goal.

Motivation for Glass Core Substrates

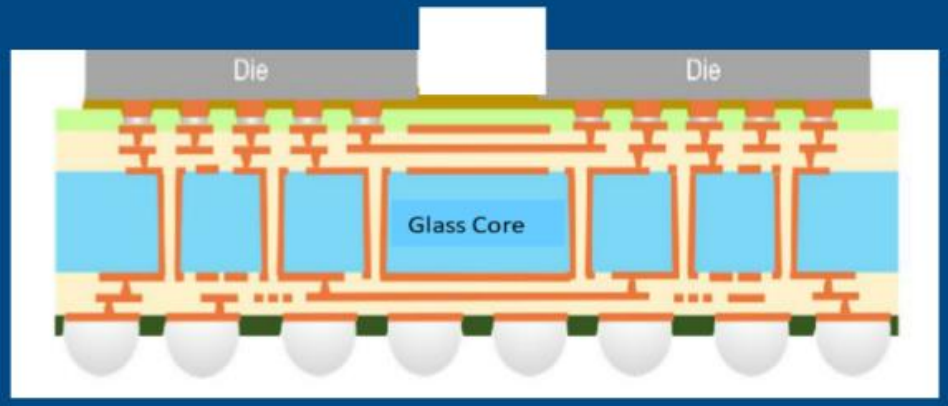
Organic Substrate



Organic substrates leverage traditional PCB-like cores with woven glass laminates

- Provides a low cost, easily manufacturable material set with off the shelf laminates available from leading suppliers

Glass Core Substrate



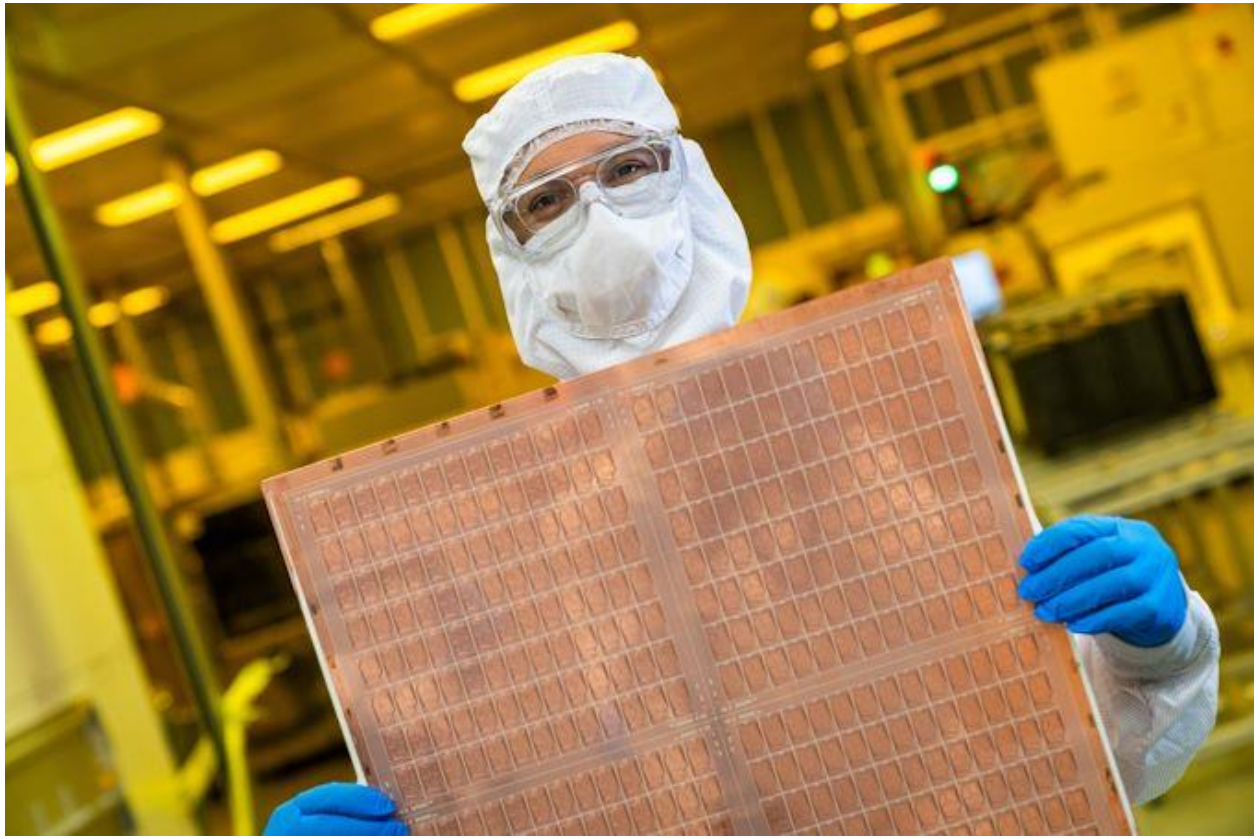
Glass core substrate enable significant improvement to both electrical and mechanical properties

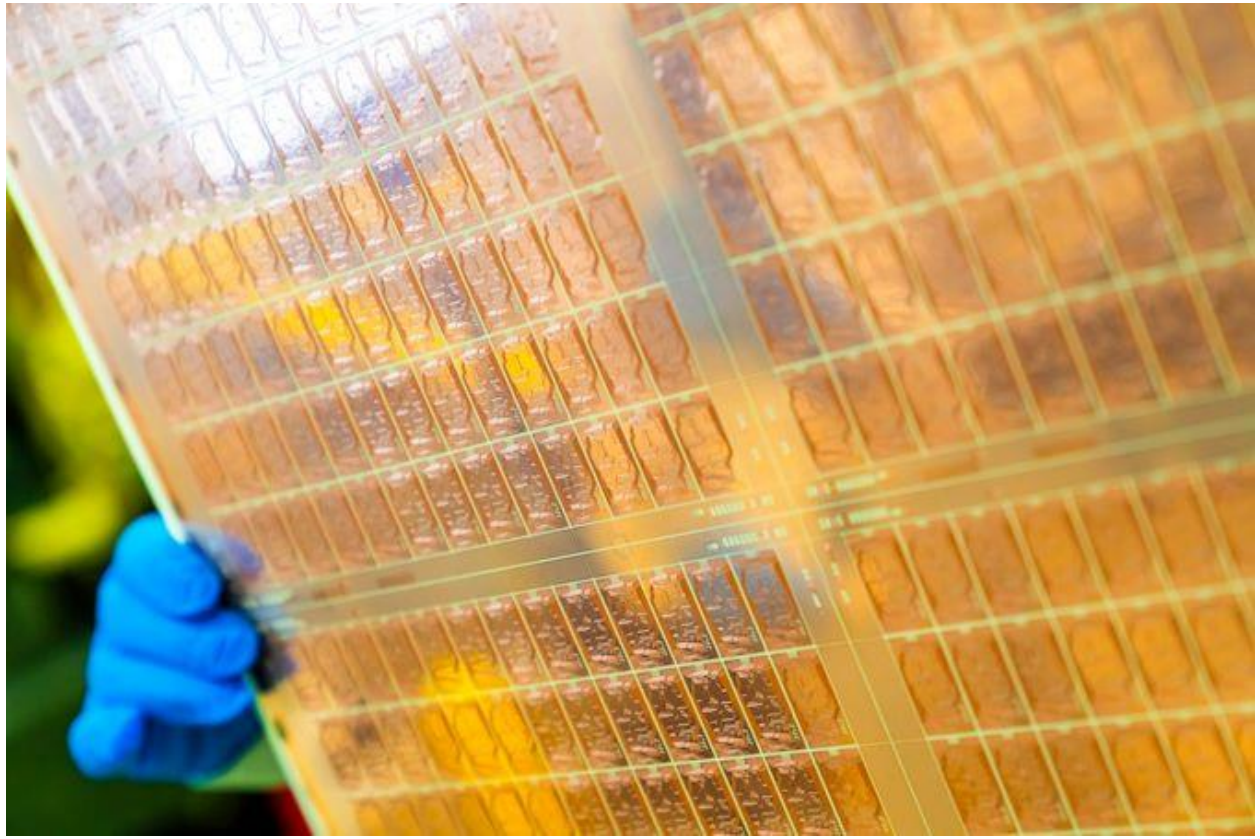
- Tunable Modulus and CTE closer to silicon → Large form factor enabling
- Dimensional stability → Improved feature scaling
- High (~10x) through-hole density → improved routing and signaling
- Low Loss → High speed signaling
- Higher Temperature capability → Advanced Integrated Power Delivery

Glass Core has similar properties as Si → Dimensional stability and ability to scale

*Based on internal analysis of Intel products and projections of future Intel products

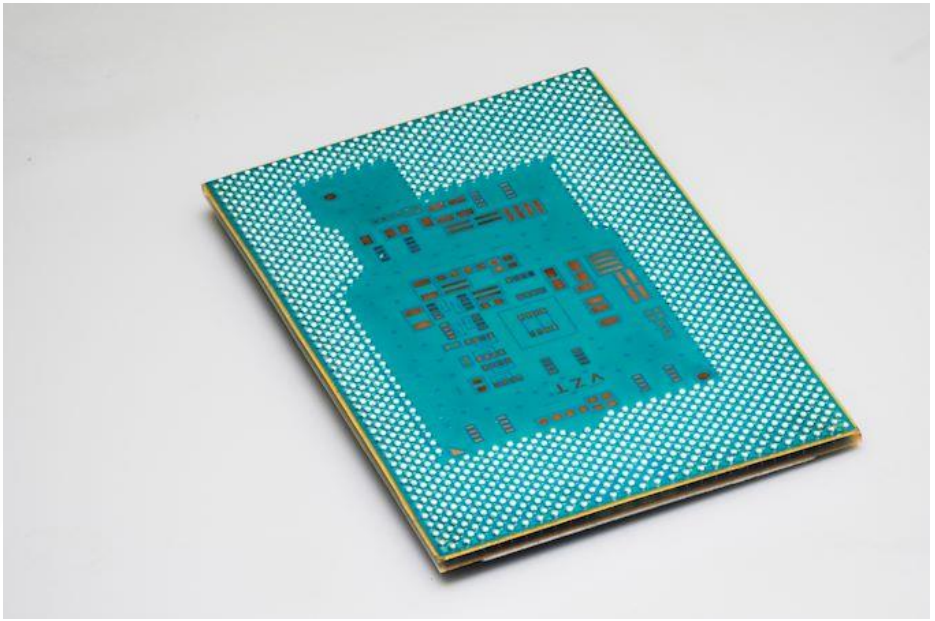
Intel Glass Panel





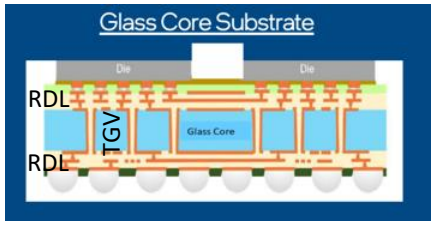
Panel size: 515mm x 510mm

Intel's Fully Functional Test Chip



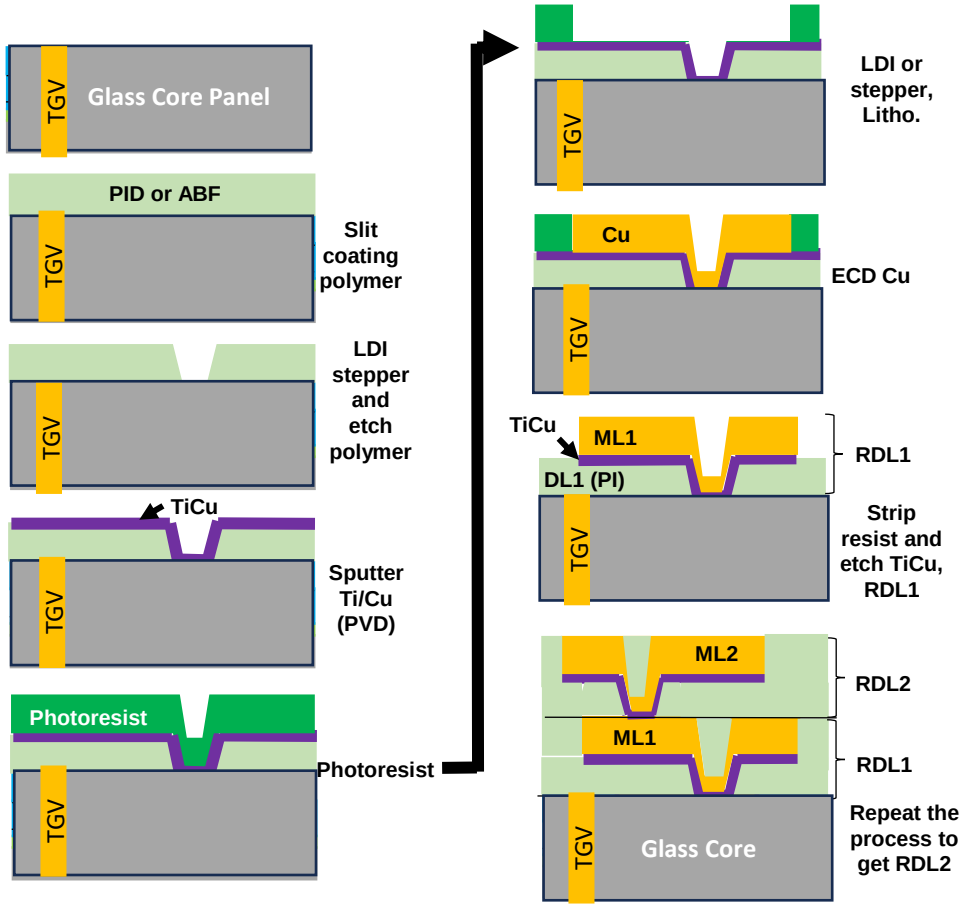
- Altogether, Intel has spent over a billion dollars on glass core R&D thus far in Chandler, Arizona.
- The glass core was made very thick – on the order of 1mm – in order to prove that TGVs would work with such a thick core.
- 3 layers of RDL, and the TGVs have a pitch of 75µm. Die-to-die bump pitch < 36µm.
- Intel claims that glass substrates allow for a much higher interconnect density (i.e., finner pitches), which is crucial for power delivery and signal routing of next-generation SiPs.
- As part of the company's broader initiative to become a world class contract foundry, Intel will be offering glass core substrates to IFS (Intel Foundry Services) customers in due time (maybe near the end of this decade).

How to Fabricate the TGV and RDLs?



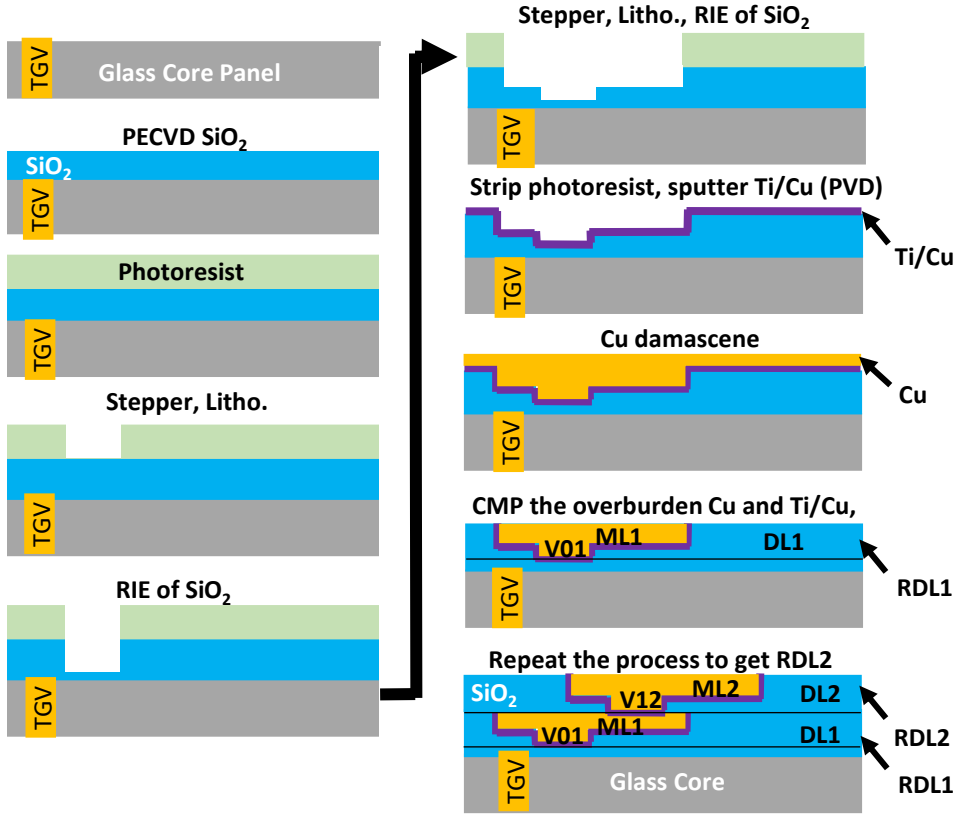
TGV (Through Glass Via) can be Fabricated by either Laser or DRIE (for finer pitch)

Fabrication of the Ordinary L/S (≧2μm) RDLs



- PID or ABF as dielectric layer (≦5μm)
- Pad pitch (≥2μm)
- LDI or Stepper
- PVD
- ECD Cu

Fabrication of the L/S (<2μm) RDLs



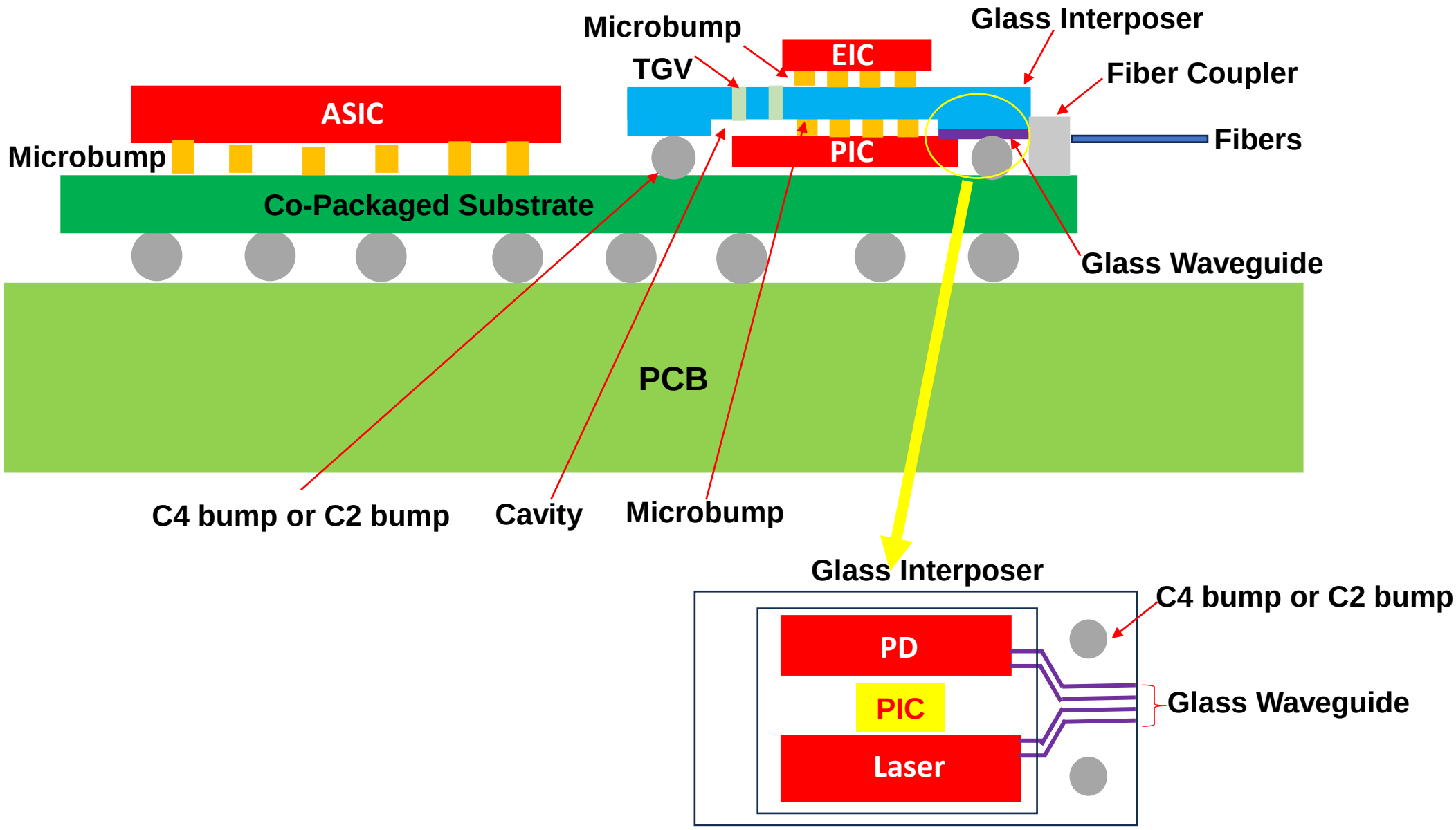
- SiO_2 as dielectric layer (~1μm)
- Pad pitch (<2μm)
- PECVD
- Stepper
- PVD
- Cu-damascene
- CMP

Challenges on Glass Substrate

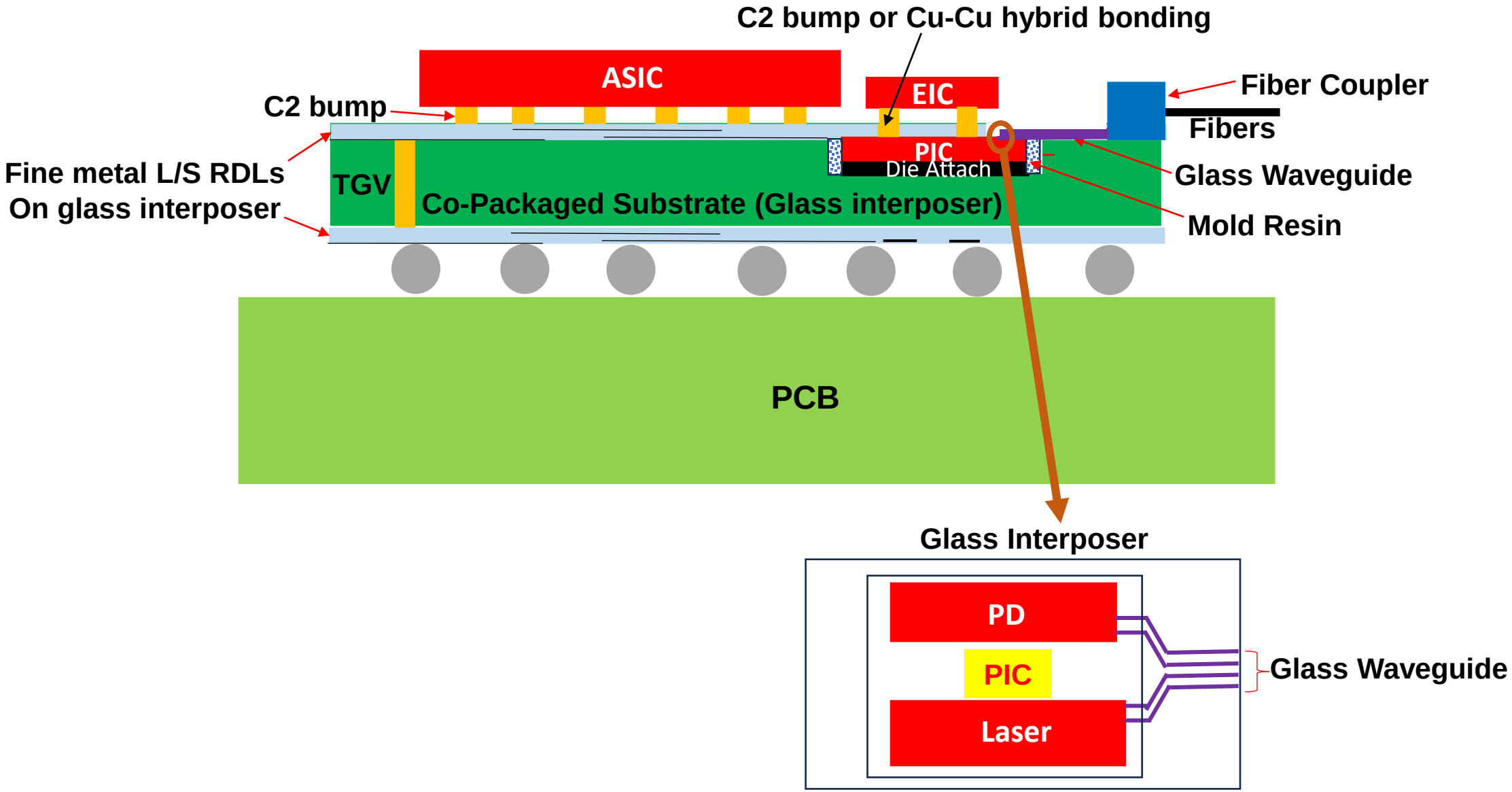
According to Ann Kelleher, executive VP of technology development at Intel:

- Glass substrates will be more expensive to produce and package than tried-and-tested organic substrates.
- There will be the yield issues at the start.
- Glass substrates will need to build a viable ecosystem for commercial production. This includes necessary tooling and supply capacity. That's why Intel is working closely with glass-handling equipment and material suppliers.
- The company will also have to find ways to outsource test and assembly of these new substrates.

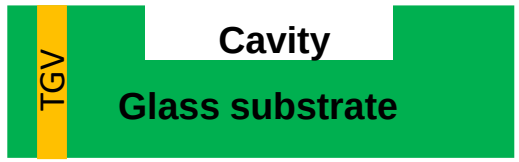
3D heterogeneous integration of EIC and PIC with a glass interposer

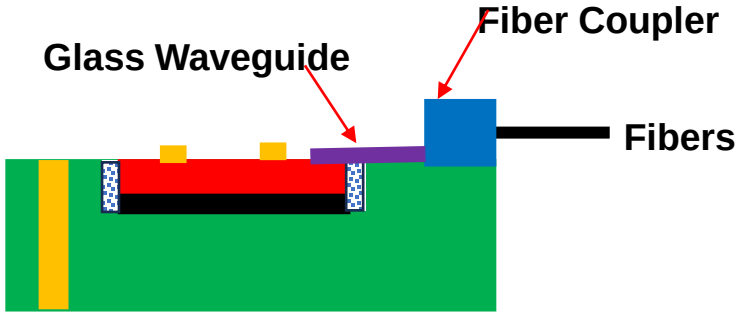


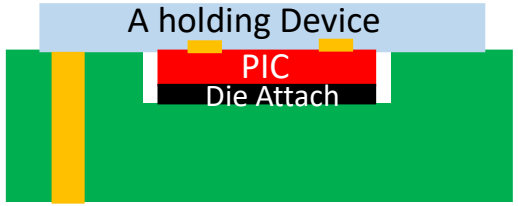
3D heterogeneous integration of ASIC, EIC and PIC on a co-packaged substrate (glass interposer)

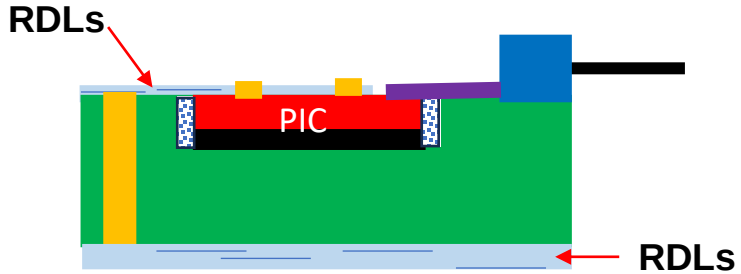


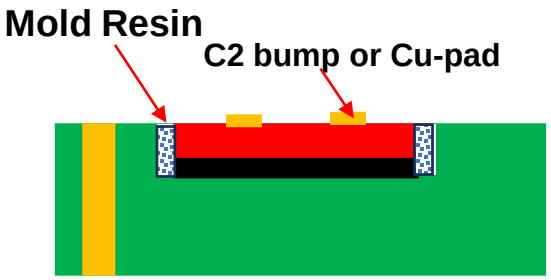
Process in fabrication of the 3D heterogeneous integration of ASIC, EIC and PIC on a co-packaged substrate (glass interposer)

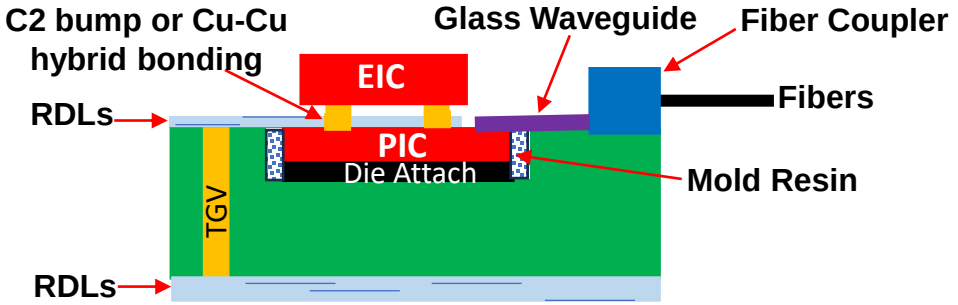












Summary

Some important results and recommendations are summarized as follows.

- **Silicon photonics are the semiconductor integration of EIC and PIC on a silicon substrate (wafer) with CMOS technology.**
- **CPO are heterogeneous integration packaging methods to integrate the OE which consists of PIC and the EE which consists of EIC as well as the switch ASIC.**
- **Roadmaps of OBO, NPO, and CPO have been provided.**
- **Various (9 different) 3D heterogeneous integrations of PIC and EIC have been proposed.**
- **Various 2D and 3D heterogeneous integrations of ASIC Switch, PIC and EIC (CPO) w/o bridge have been proposed.**
- **Various heterogeneous integration of ASIC Switch, PIC and EIC (CPO) on glass substrate have been proposed.**

Some Recent Advanced Packaging Papers Published by the Lecturer and his Colleagues

1. Lau, J. H., "State-of-the-art of Cu-Cu Hybrid Bonding", *IEEE Transactions on CPMT*, Vol. 14, No. 3, March 2024.
2. Lau, J. H., "Co-Packaged Optics - Heterogeneous Integration of Photonic IC and Electronic IC", *IEEE Transactions on CPMT*, Vol. 14, No. 3, March 2024.
3. Lau, J. H, C. Lin, et al., "Hybrid Substrate with Ultra-Large Organic Interposer for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 13, No. 9, September 2023.
4. Lau, J. H, G. Chen, et al., "Hybrid Substrates for Heterogeneous Integration" *ASME Transactions, Journal of Electronic Packaging*, published online: August 11, 2023.
5. Lau, J. H., "Recent Advances and Trends in Chiplet Design and Heterogeneous Integration Packaging", *ASME Transactions, Journal of Electronic Packaging*, published online: June 23, 2023.
6. Lau, J. H., "Recent Advanced and Trends in Cu-Cu Hybrid Bonding", *IEEE Transactions on CPMT*, Vol. 13, No. 3, March 2023, pp. 399-425.
7. Lau, J. H., "Recent Advanced and Trends in Multiple system and Heterogenous Integration with TSV-Interposers", *IEEE Transactions on CPMT*, Vol. 13, No. 1, January 2023, pp. 3-25.
8. Lau, J. H., "Recent Advanced and Trends in Multiple system and Heterogenous Integration with TSV-less Interposers", *IEEE Transactions on CPMT*, Vol. 12, No. 8, August 2022, pp. 1271-1280.
9. Lau, J. H., "Recent Advances and Trends in Advanced Packaging", *IEEE Transactions on CPMT*, Vol. 12, No. 2, February 2022, pp. 228-252.
10. Lau, J. H., G. Chen, J. Huang, et al., "Hybrid Substrate by Fan-Out RDL-First Panel-Level Packaging, *IEEE Transactions on CPMT*, Vol. 11, No. 8, August 2021, pp. 1301-1309.
11. Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", *ASME Transactions, Journal of Electronic Packaging*, Vol. 143, June 2021, pp. 1-36.
12. Lau, J. H., C. Ko, C. Lin, et al., "Fan-Out Panel-Level Packaging of Mini-LED RGB Display", *IEEE Transactions on CPMT*, Vol. 11, No. 5, May 2021, pp. 739-747.
13. Lau, J. H., C. Ko, K. Yang, et al., "Panel-Level Fan-Out RDL-first Packaging for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1125-1137.
14. Lau, J. H., C. Ko, T. Tseng, et al., "Panel-Level Chip-Scale Package with Multiple Diced Wafers", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1110-1124.
15. Lau, J. H., "Recent Advances and Trends in Fan-Out Wafer/Panel-Level Packaging", *ASME Transactions, Journal of Electronic Packaging*, Vol. 141, December 2019, pp. 1-27.
16. Lau, J. H., M. Li, M. Li, et al., "Fan-out wafer-level packaging for heterogeneous integration," *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.
17. Lau, J. H., M. Li, Q. Li, et al., "Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging*", IEEE Transactions on CPMT.* Vol. 8, Issue 6, June 2018, pp. 991-1002.
18. Lau, J. H., M. Li, Y. Li, et al., "Warpage Measurements and Characterizations of FOWLP with Large Chips and Multiple RDLs", *IEEE Transactions on CPMT*, Vol. 8, Issue 10, October 2018, pp. 1729-1737.
19. Lau, J. H., M. Li, D. Tian, et al., "Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT*, Vol. 7, Issue 10, October 2017, pp. 1729-1738.
20. Lau, J. H., "Recent Advances and New Trends in Flip Chip Technology", *ASME Transactions, Journal of Electronic Packaging*, September 2016, Vol. 138, Issue 3, pp. 1-23.
21. Lau, J. H., Q. Zhang, M. Li, et al., "Stencil Printing of Underfill for Flip Chips on Organic-Panel and Si-Wafer Substrates", *IEEE Transactions on CPMT*, Vol. 5, No. 7, July 2015, pp. 1027-1035.
22. Lau, J. H., "Overview and Outlook of 3D IC Packaging, 3D IC Integration, and 3D Si Integration", *ASME Transactions, Journal of Electronic Packaging*, December 2014, Vol. 136, Issue 4, pp. 1-15.
23. Lau, J. H., C. Lee, C. Zhan, et al., "Low-Cost Through-Silicon Hole Interposers for 3D IC Integration", *IEEE Transactions on CPMT*, Vol. 4, No. 9, September 2014, pp. 1407-1419.

Some Packaging Books Published by the Lecturer and his Colleagues

1. Lau, J. H., *Flip Chip, Hybrid Bonding, Fan-in, and Fan-out Technology*, Springer, new York, 2024.
2. Lau, J. H., *Chiplet Design and Heterogeneous Integration Packaging*, Springer, New York, 2023.
3. Lau, J. H., *Semiconductor Advanced Packaging*, Springer, New York, 2021.
4. Lau, J. H., and N. C. Lee, *Assembly and Reliability of Lead-Free Solder Joints*, Springer, New York, 2020.
5. Lau, J. H., *Heterogeneous Integrations*, Springer, New York, 2019.
6. Lau, J. H., *Fan-Out Wafer-Level Packaging*, Springer, New York, 2018.
7. Lau, J. H., *3D IC Integration and Packaging*, McGraw-Hill, New York, 2016.
8. Lau, J. H., *Through-Silicon Via (TSV) for 3D Integration*, McGraw-Hill, New York, 2013.
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10. Lau, J. H., C. K. Lee, C. S. Premachandran, and Yu Aibin, *Advanced MEMS Packaging*, McGraw-Hill, New York, 2010.
11. Lau, J. H., C. P. Wong, N. C. Lee, and R. Lee, *Electronics Manufacturing with Lead-Free, Halogen-Free, and Adhesive Materials*, McGraw-Hill, New York, 2003.
12. Lau, J. H., and R. Lee, *Microvias for Low Cost, High Density Interconnects*, McGraw-Hill, New York, 2001.
13. Lau, J. H., *Low Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies*, McGraw-Hill, New York, 2000.
14. Lau, J. H., and R. Lee, *Chip Scale Package: Design, Materials, Process, Reliability, and Applications*, McGraw-Hill, New York, 1999.
15. Lau, J. H., C. P. Wong, J. Prince, and W. Nakayama, *Electronic Packaging: Design, Materials, Process, and Reliability*, McGraw-Hill, New York, 1998.
16. Lau, J. H., and Y. Pao, *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies*, McGraw-Hill, New York, 1997.
17. Lau, J. H., (editor) *Flip Chip Technologies*, McGraw-Hill, New York, 1996.
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Thank You Very Much for Your Attention!