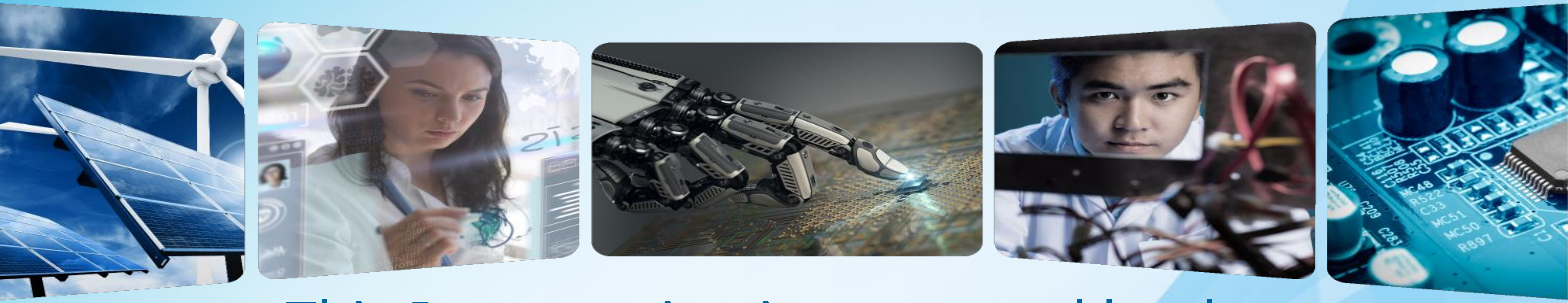
Chitpet Design and Heterogeneous Integration Packaging

(For IEEE/EPS Toronto Chapter)

John H Lau
Unimicron Technology Corporation
John_Lau@unimicron.com



This Presentation is supported by the IEEE Electronics Packaging Society’s Distinguished Lecturer Program

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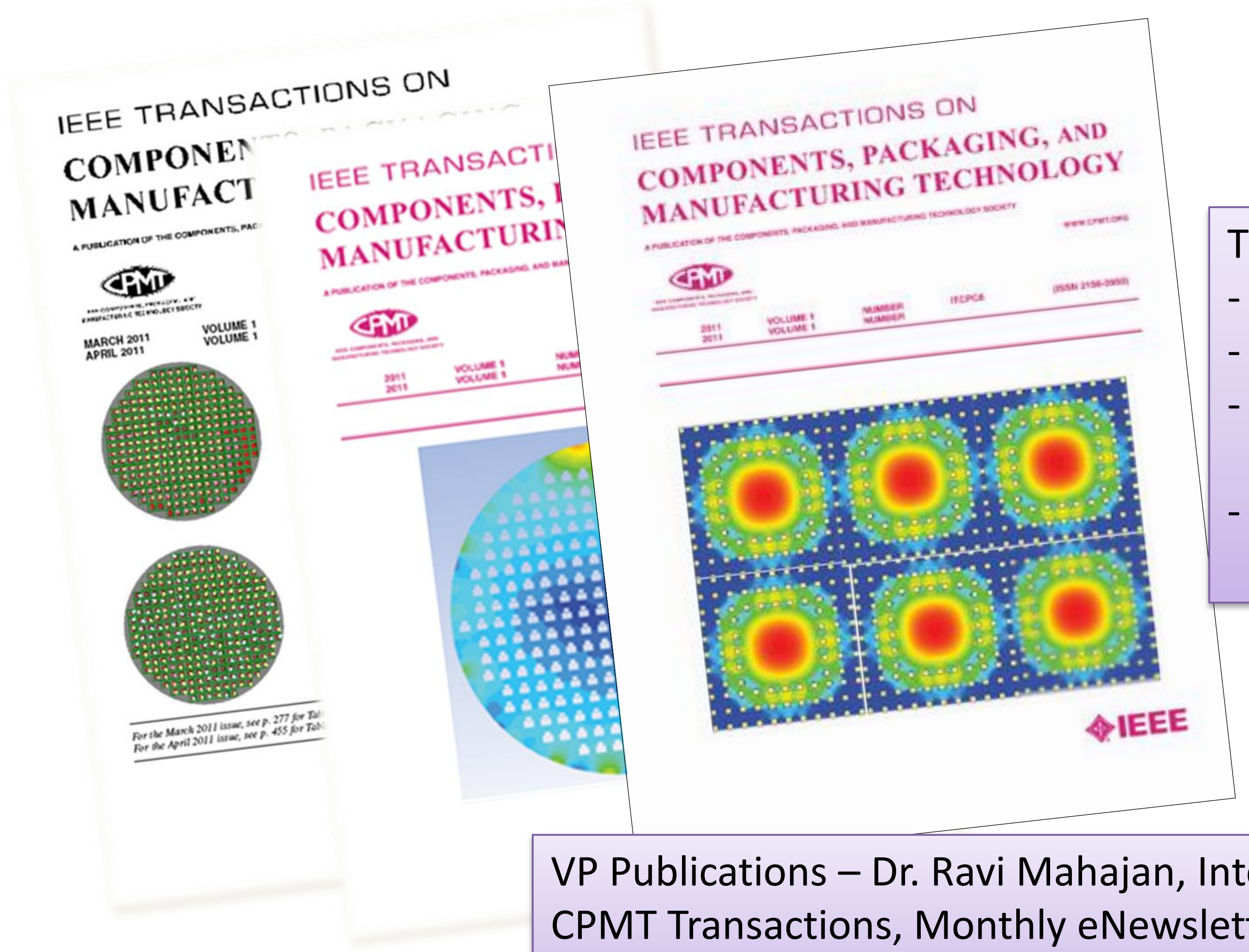

Transactions on CPMT

- 595 submissions (2020)
- 240 papers published
- Impact Factor: ~ 1.7 (2020)
- Xplore Usage: 40,000+

VP Publications – Dr. Ravi Mahajan, Intel
CPMT Transactions, Monthly eNewsletter, and Bi-Annual printed Newsletter

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IEEE Electronics Packaging Award
(IEEE Technical Field Award)

Outstanding Sustained Technical Contribution Award

Electronics Manufacturing Technology

David Feldman Outstanding Contribution

Exceptional Technical Achievement

Outstanding Young Engineer

Transactions Best Papers

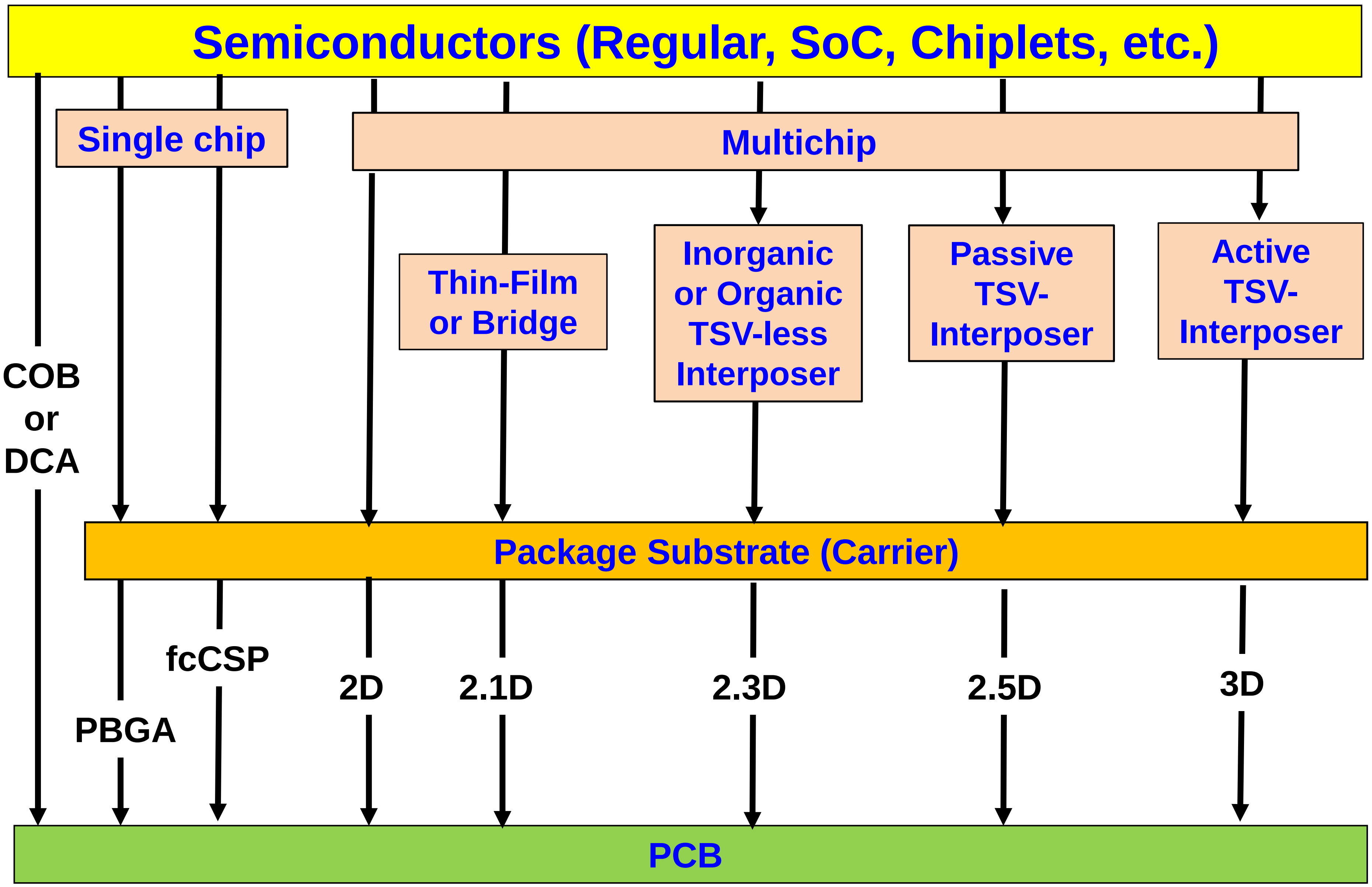
Regional Contributions

PhD Fellowship

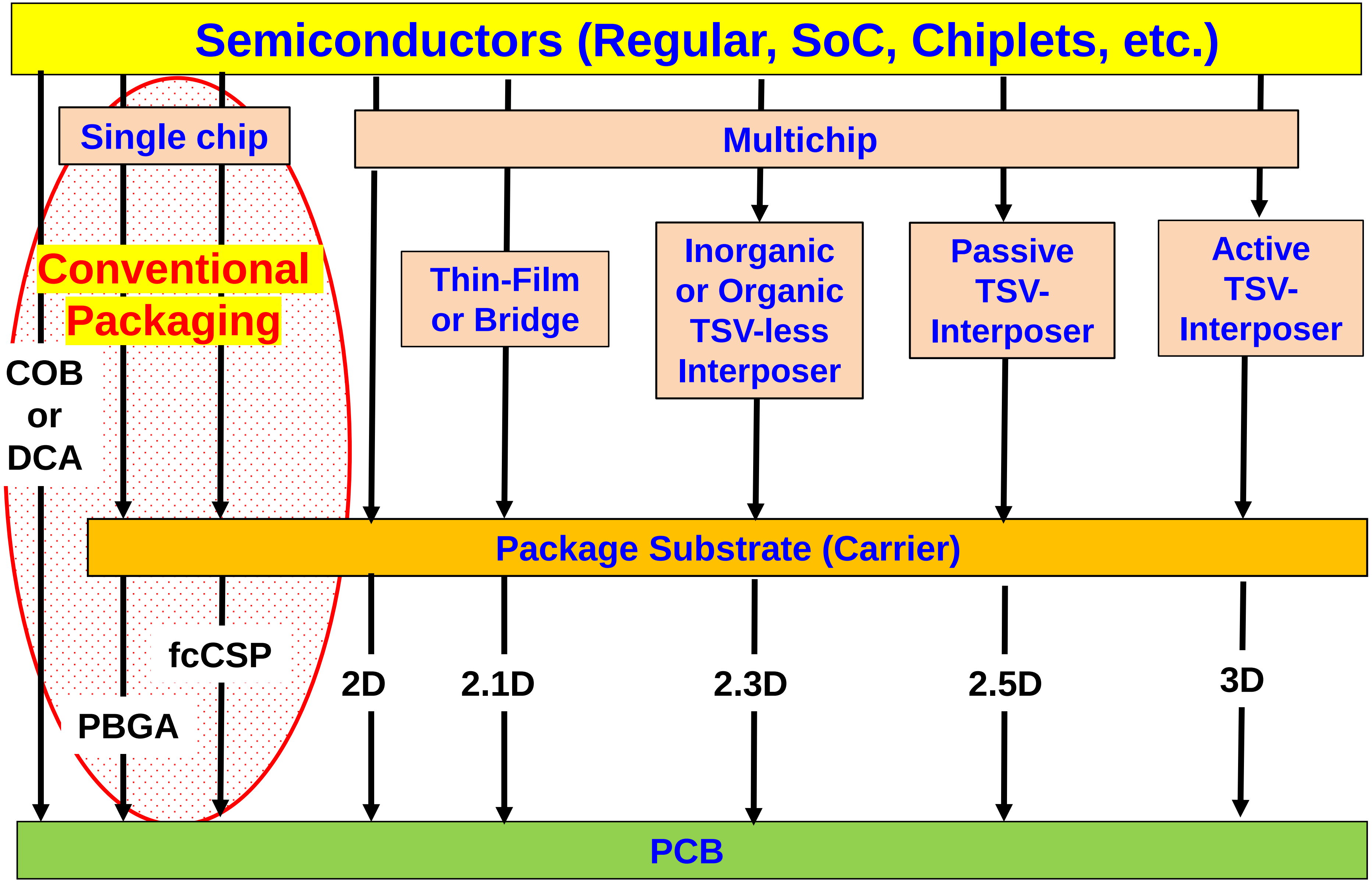
IEEE ELECTRONICS PACKAGING SOCIETY

CONTENTS

Semiconductor Packaging Technologies



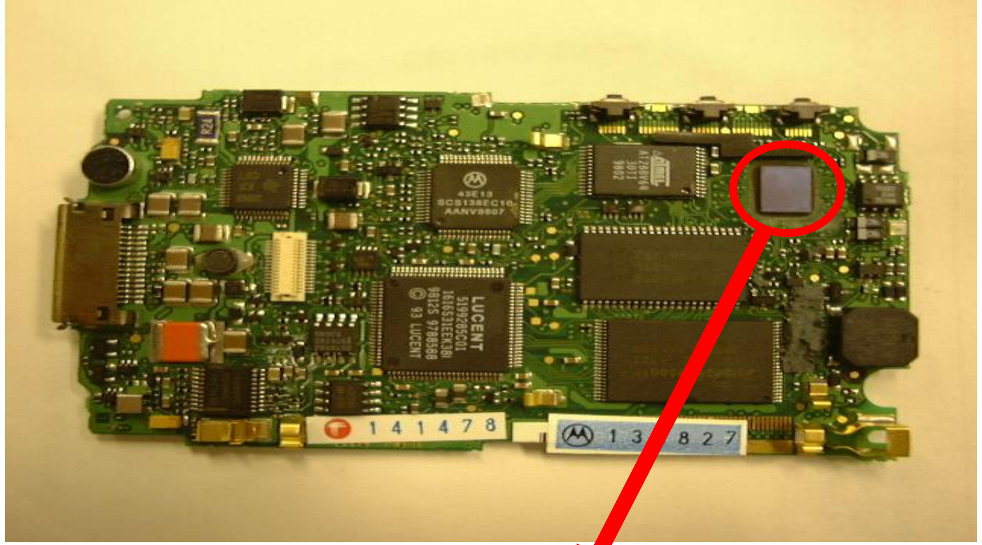
Semiconductor Packaging Technologies

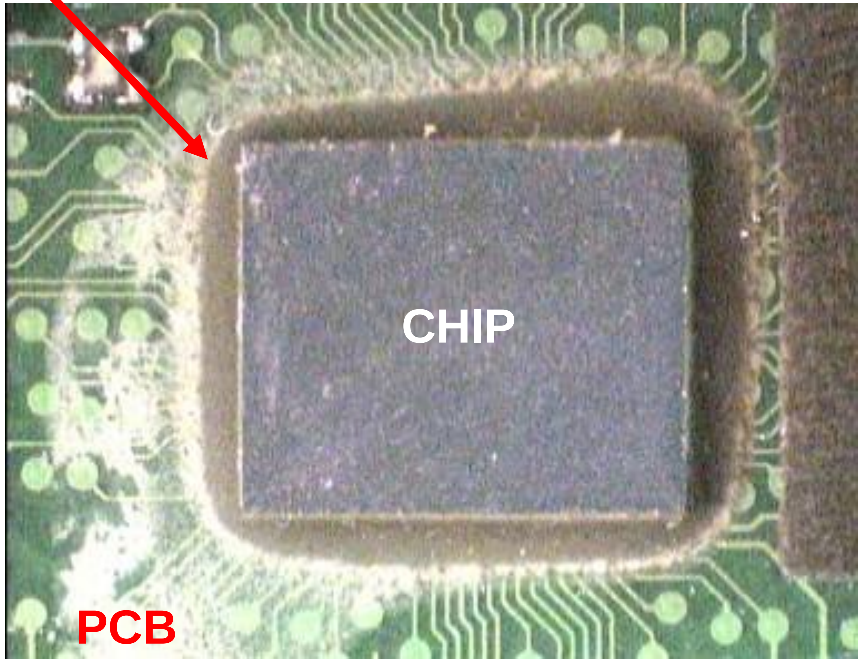


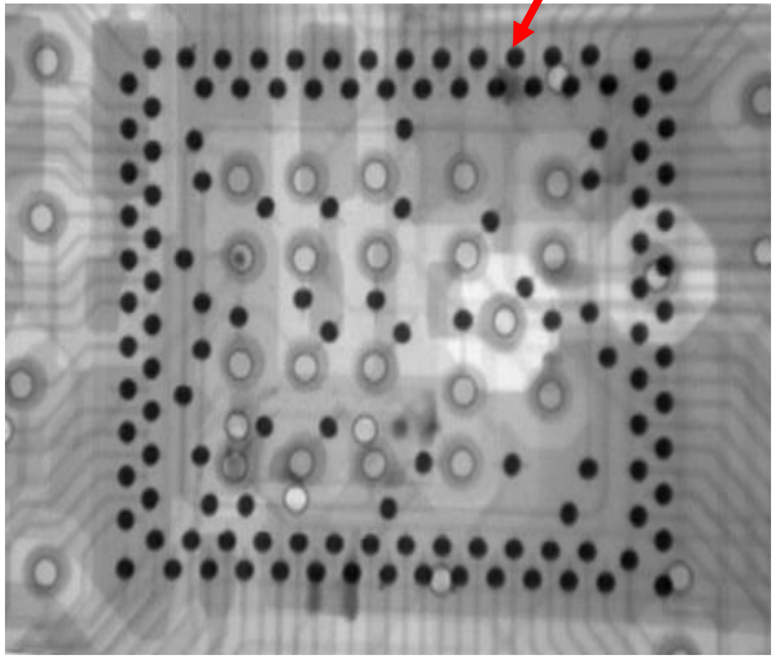
Conventional Packaging

- Direct Chip Attach
- Flip Chip Ball Grid Array

Direct Chip Attach (DCA)

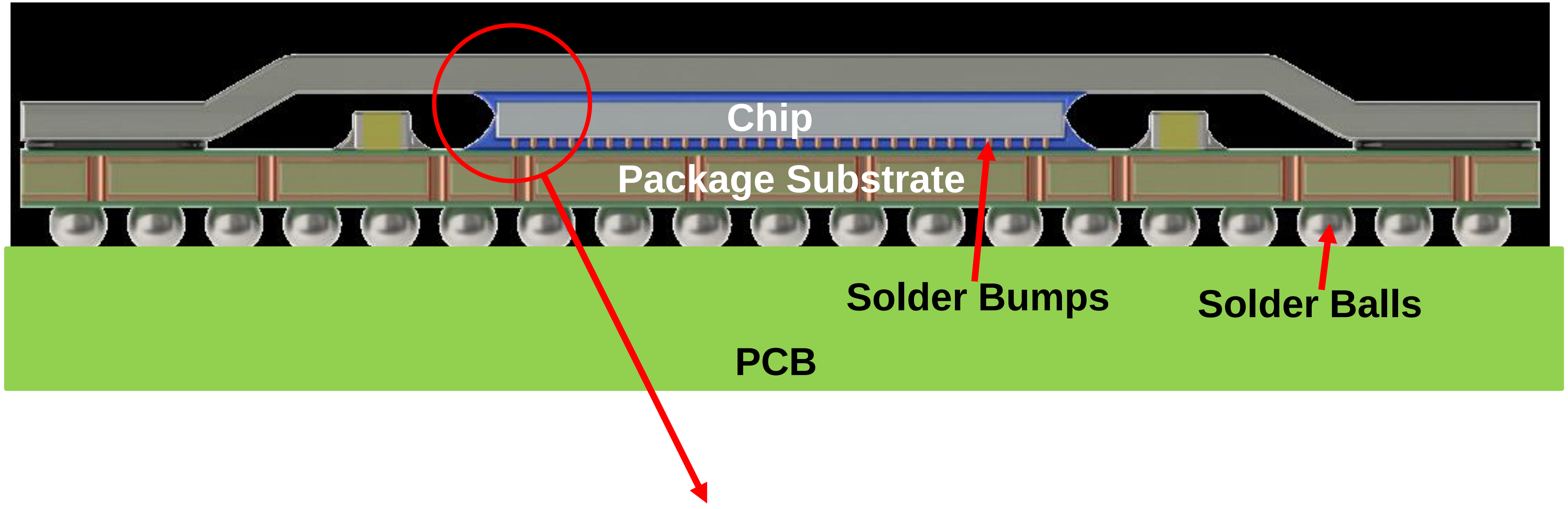


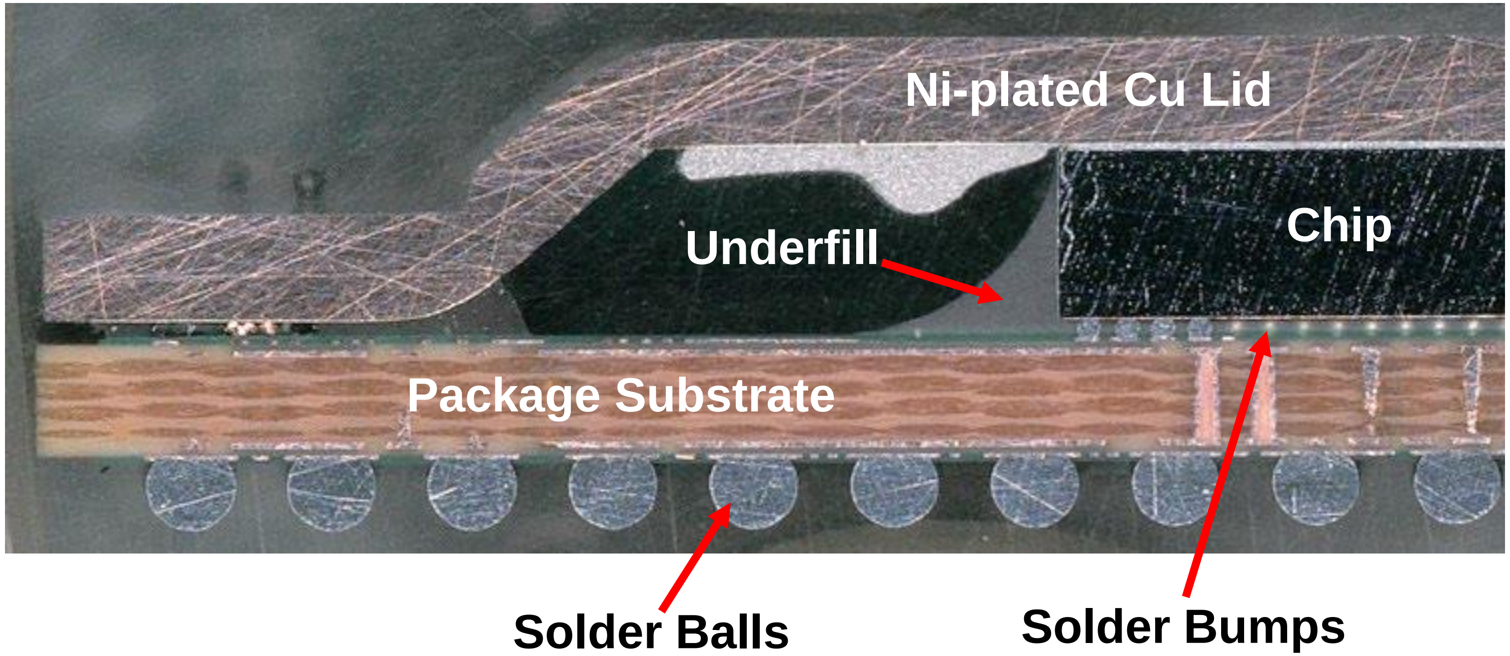




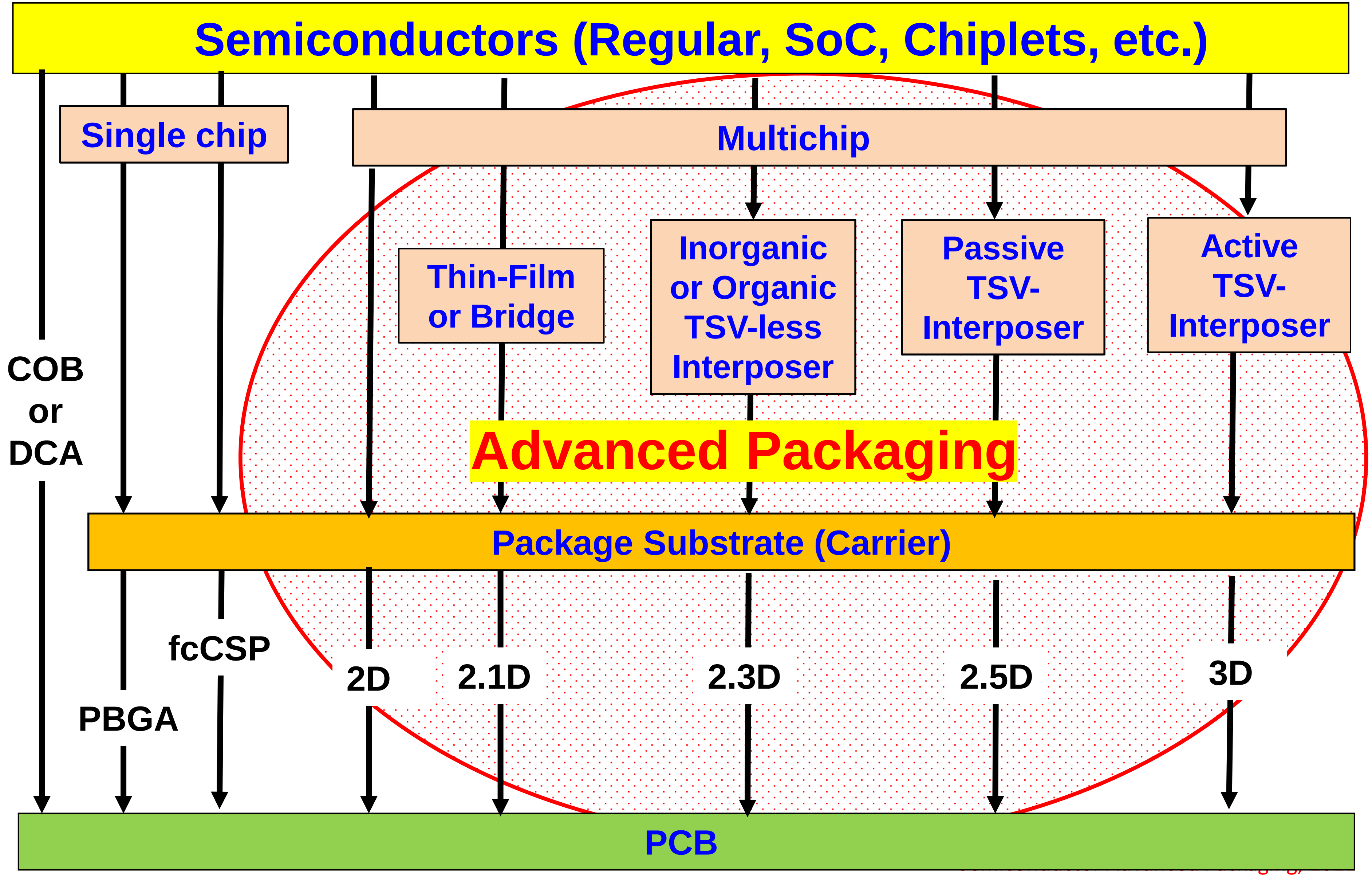
X-ray showing solder joints

Flip Chip Ball Grid Array (PBGA)





Groups of Advanced Packaging:
2D, 2.1D, 2.3D, 2.5D, and 3D IC integration



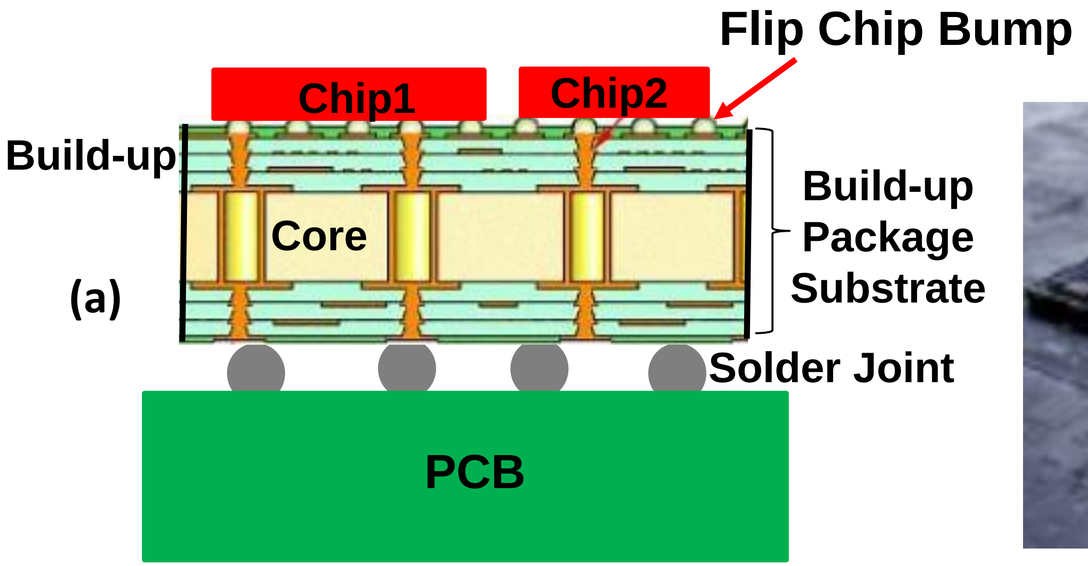
Advanced Packaging

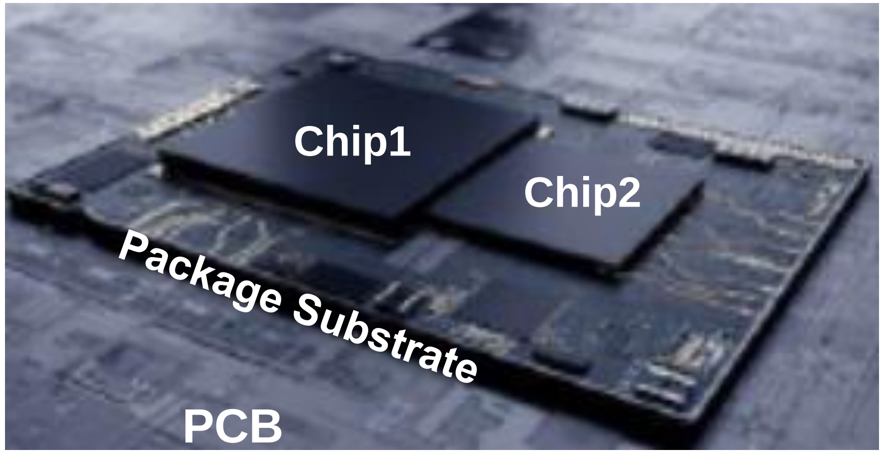
- 2D IC Integration
- 2.1D IC Integration
- 2.3D IC Integration
- 2.5D IC Integration
- 3D IC Integration

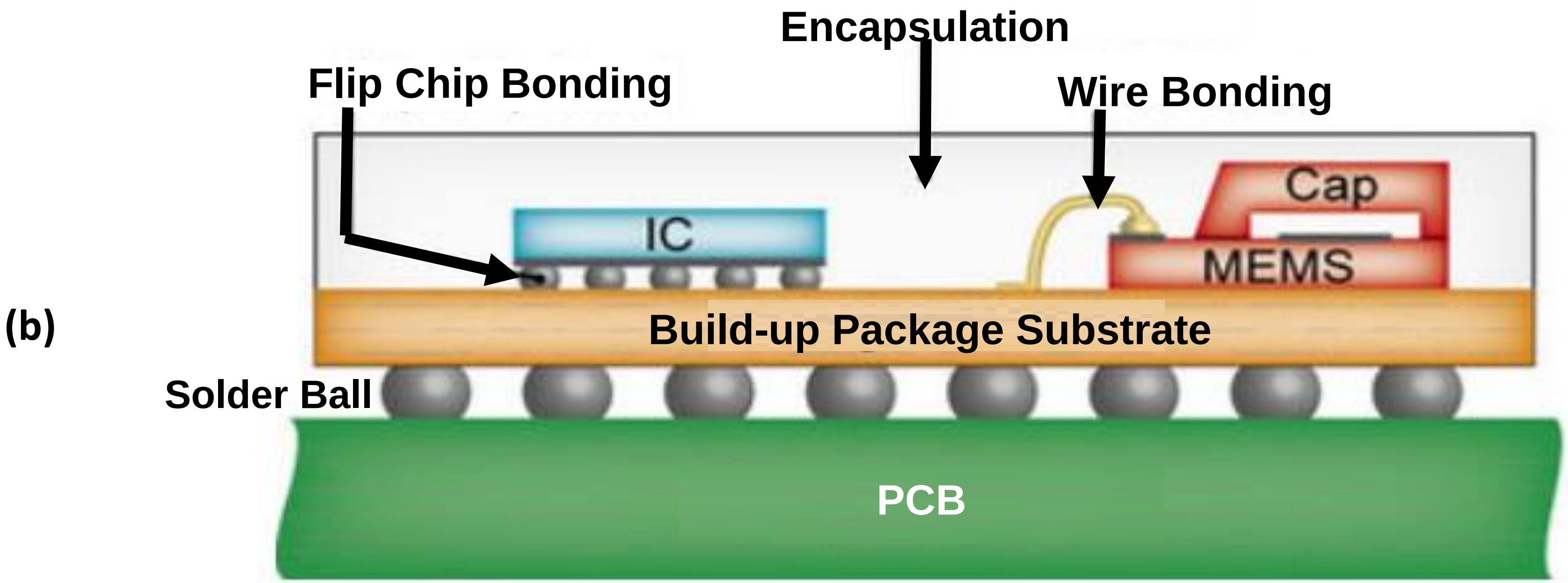
2D IC Integration

- 2D (Flip Chip) IC Integration
- 2D (Fan-Out) IC Integration
  - Flip Chip Technology
  - Fan-Out Technology
  - Antenna-in-Package (AiP)

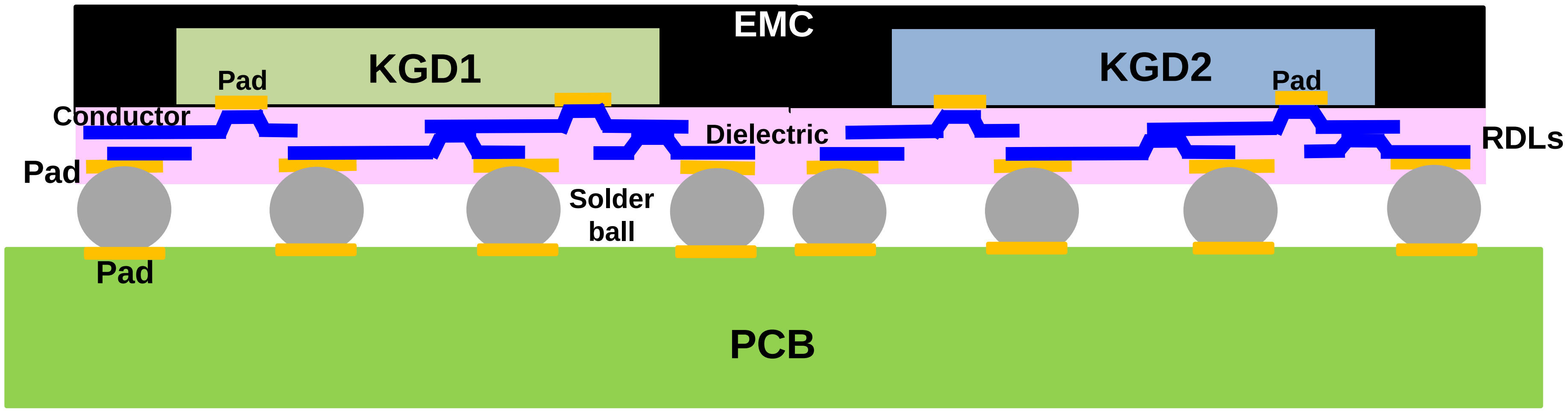
2D (Flip Chip / Wirebond) IC Integration

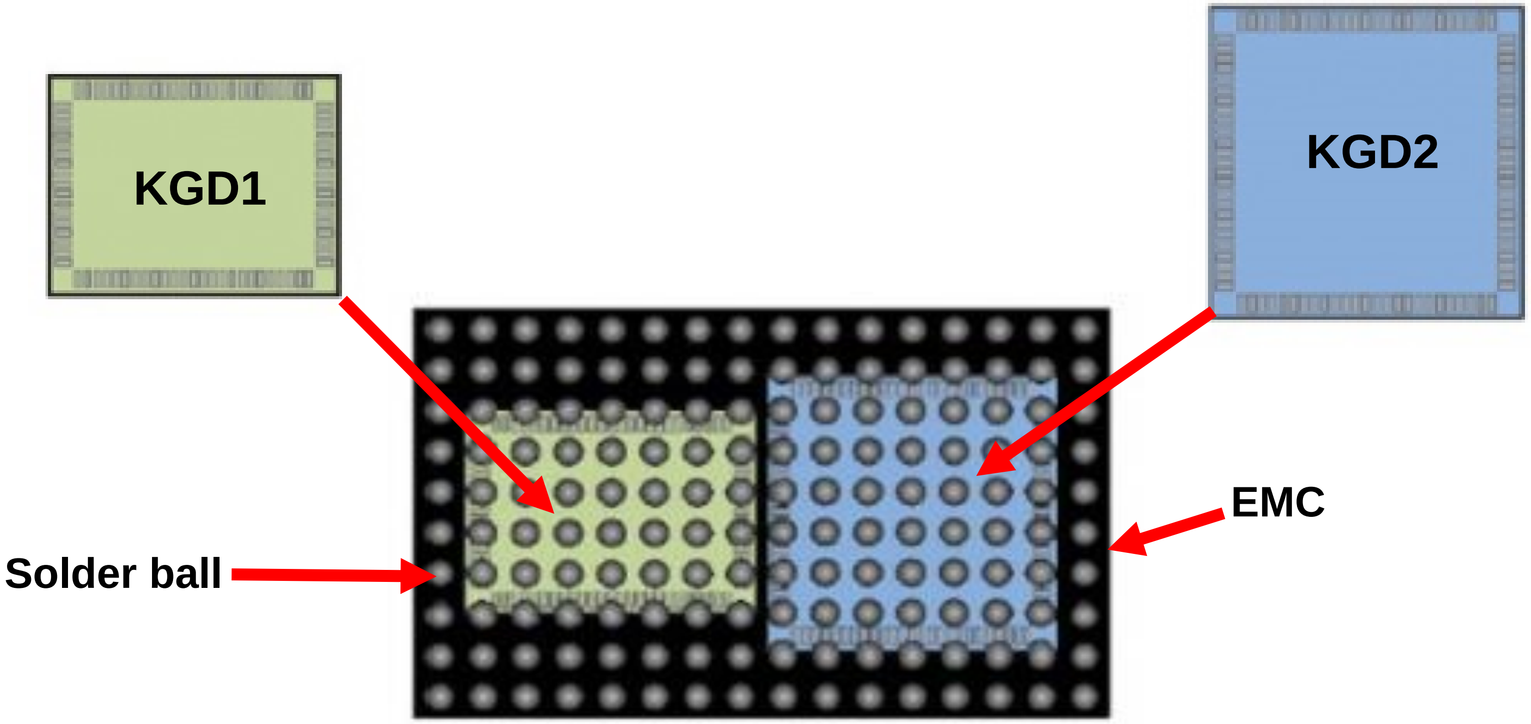






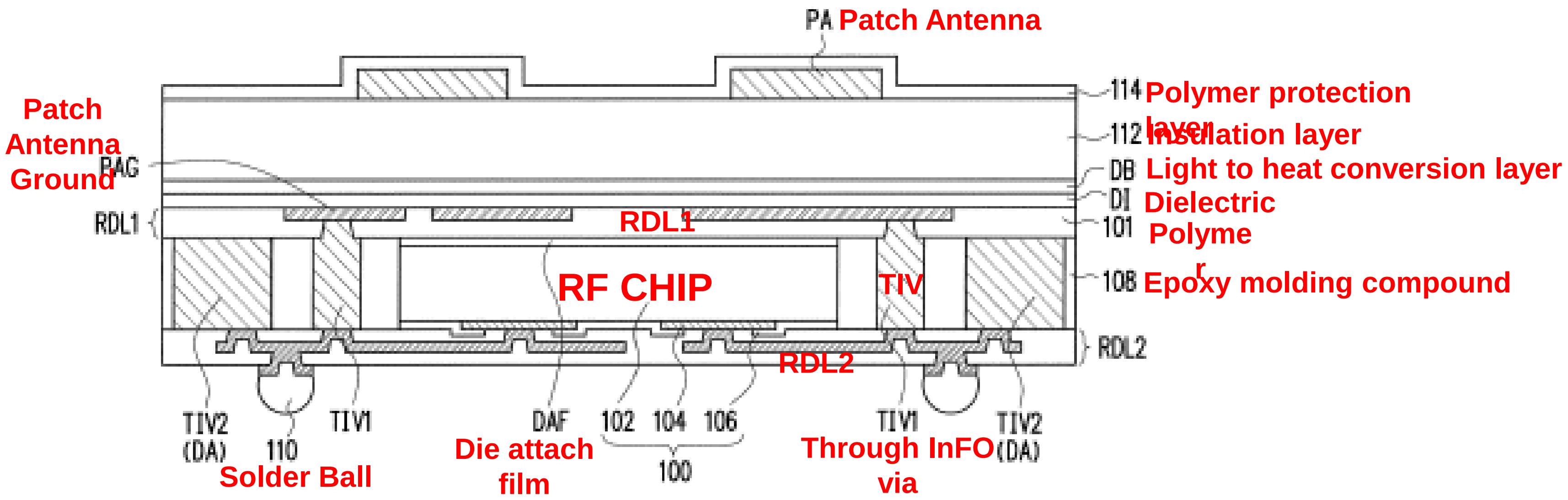
2D (Fan-Out) IC Integration





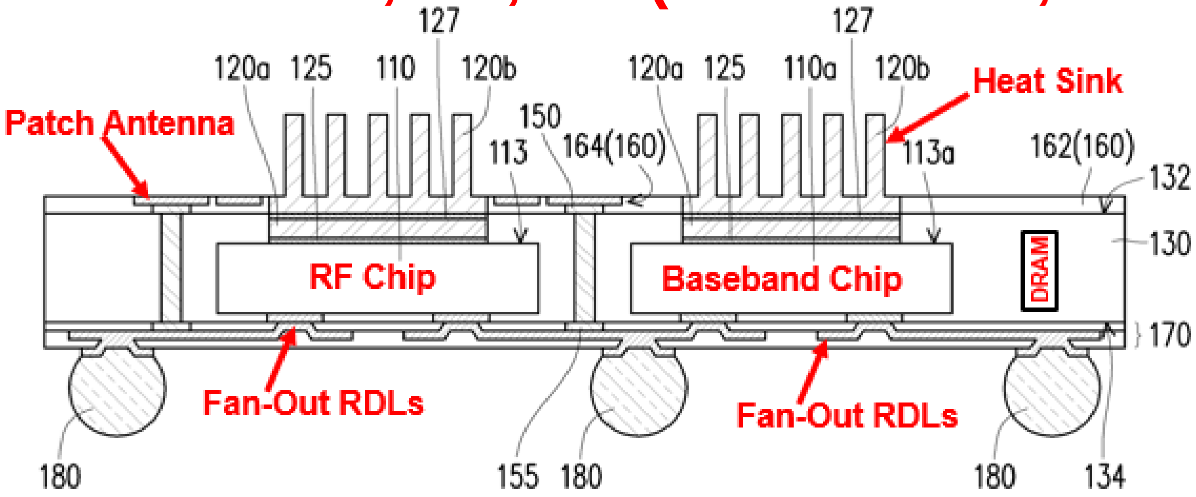
Journal of Electronic Packaging, DEC 2019

TSMC's AiP Patent: US 10,312,112 (June 4, 2019)



Fan-Out chip-first die Face-Up Process

Unimicron's Heterogeneous Integration of Baseband and AiP Patent: TW 1,209,218 (November 1, 2020)

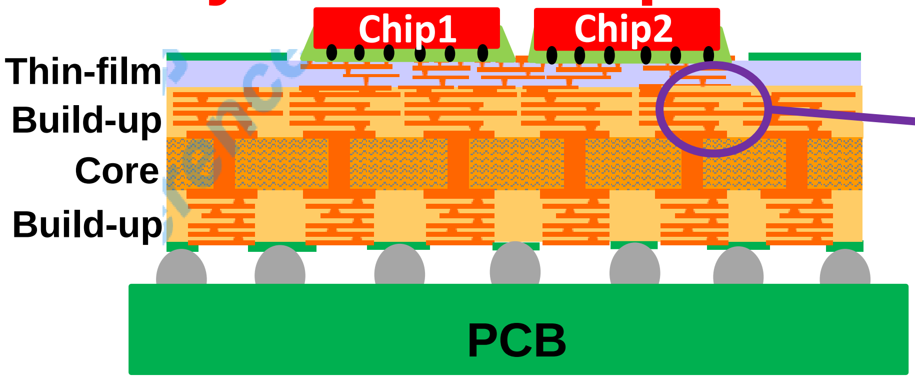


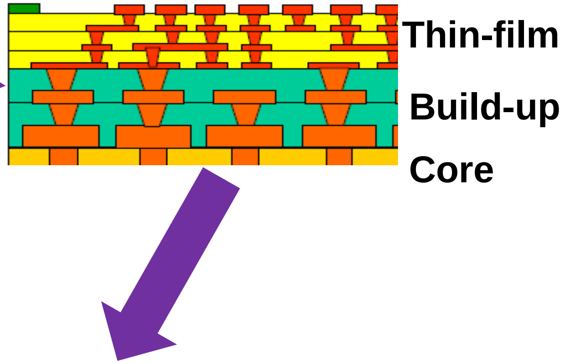
Fan-Out chip-first die Face-Down Process

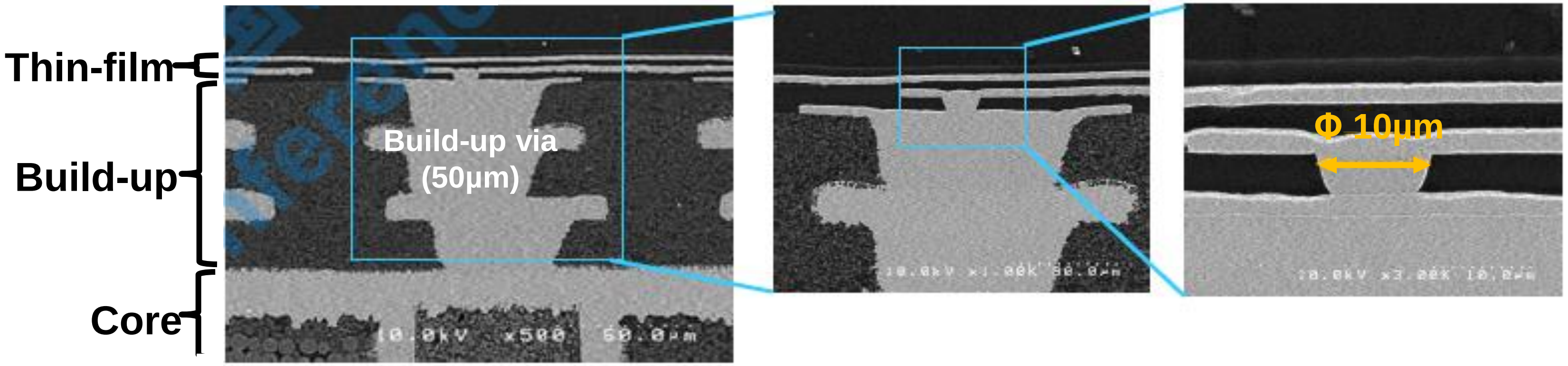
2.1D IC Integration

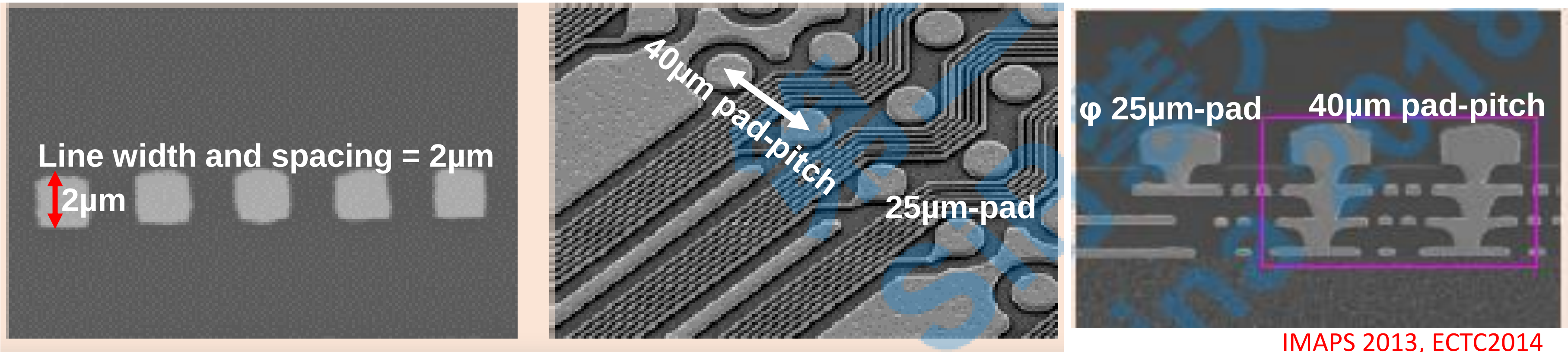
- Shinko’s integrated thin-film high-density organic package (i-THOP)
- JECT’s ultra format organic substrate (uFOS)

2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (Shinko)







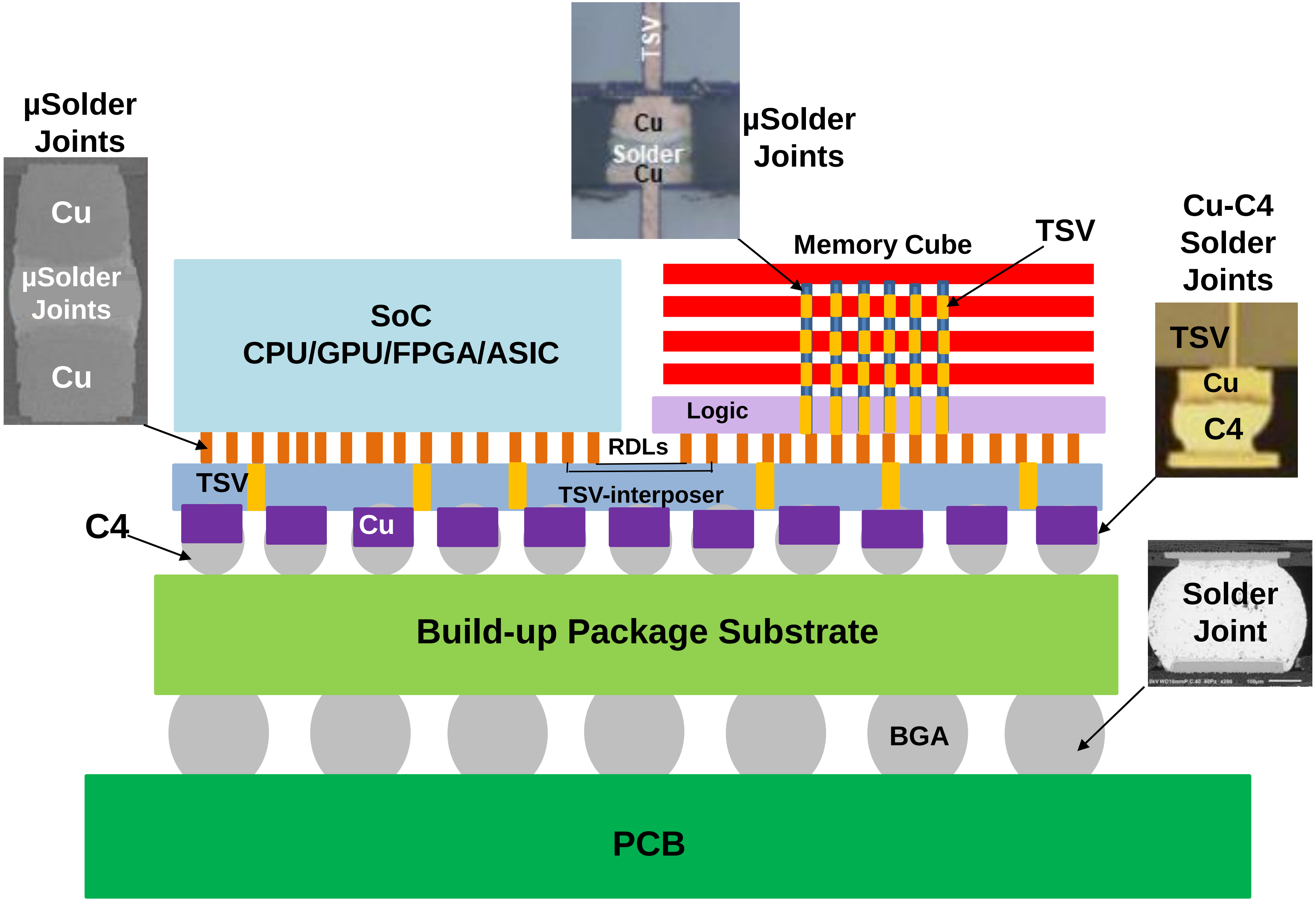


IMAPS 2013, ECTC2014

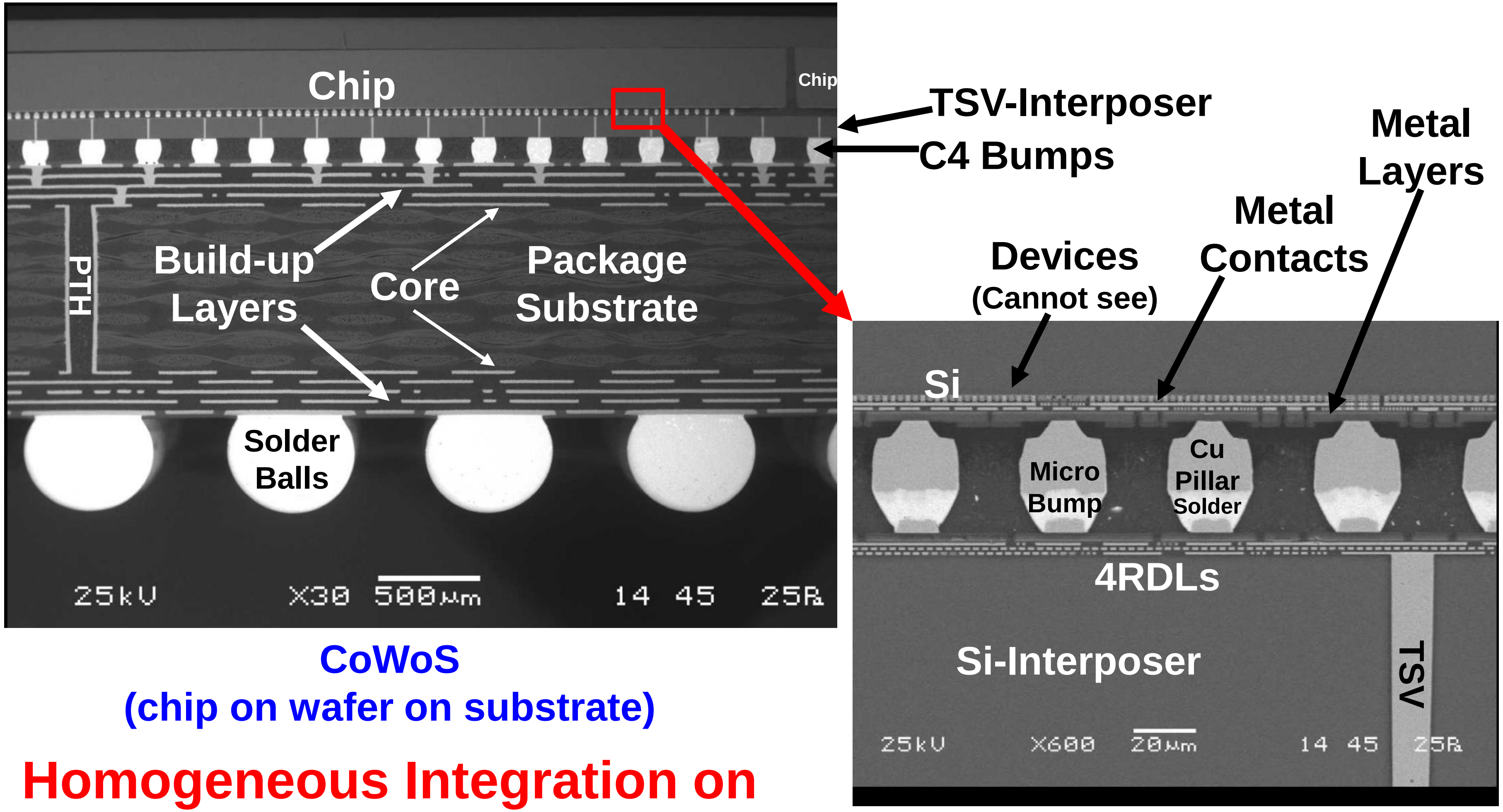
2.5D IC Integration

- Examples: TSMC, Xilinx, AMD, Nvidia, Samsung
- 2.5D for heterogeneous integration of PIC (photonic IC) and EIC (electronic IC)
- TSV and RDL manufacturing process
- TSV-less 2.5D by Samsung

2.5D IC Integration



Xilinx/TSMC's 2.5D IC Integration with FPGA



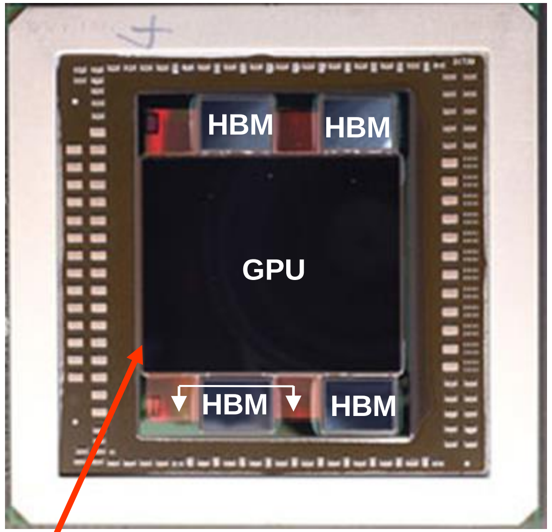
CoWoS
(chip on wafer on substrate)

Homogeneous Integration on Si-substrate

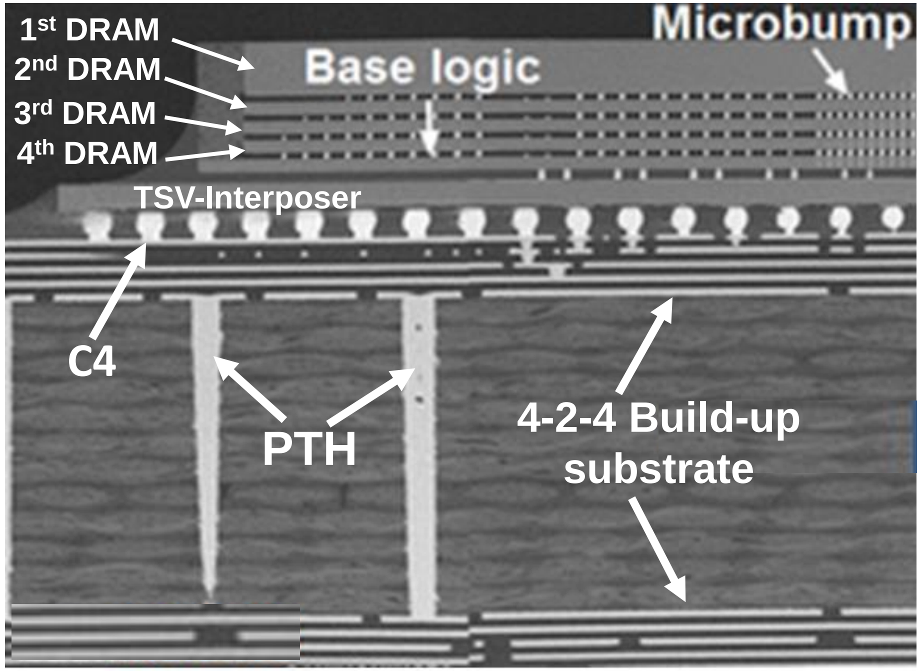
- RDLs: 0.4µm-pitch line width and spacing
- Each FPGA has >50,000 µbumps on 45µm pitch
- Interposer is supporting >200,000 µbumps

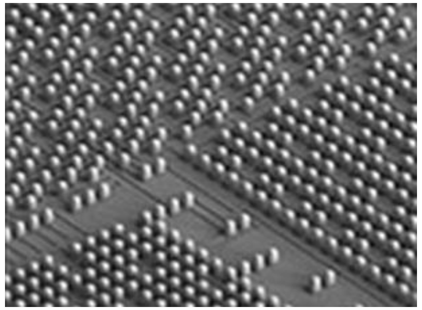
IEEE/ECTC2013

AMD's GPU (Fiji), Hynix's HBM, and UMC's Interposer

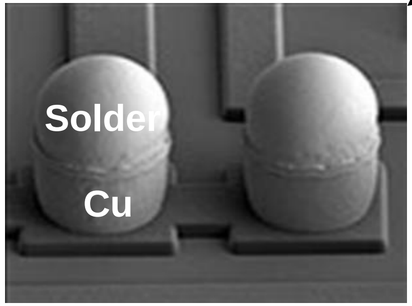


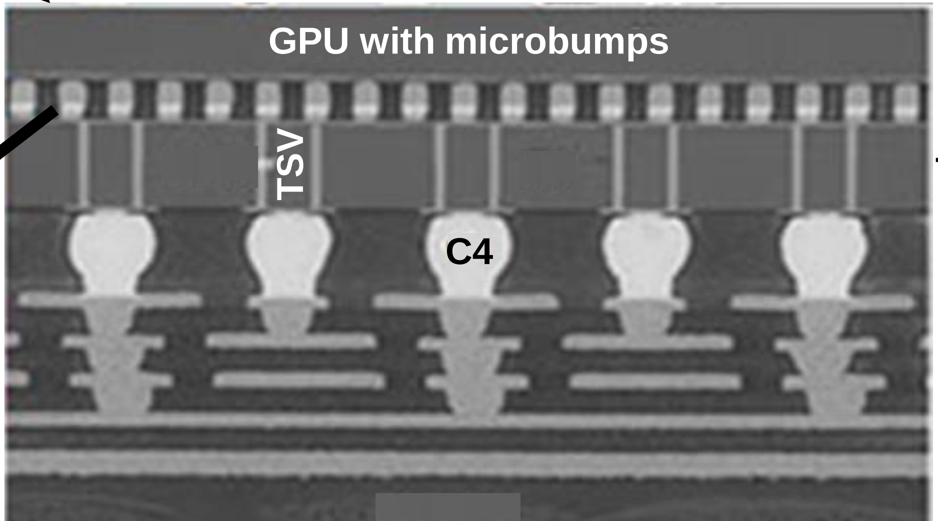
TSV-Interposer





Cu-Pillar with solder Cap



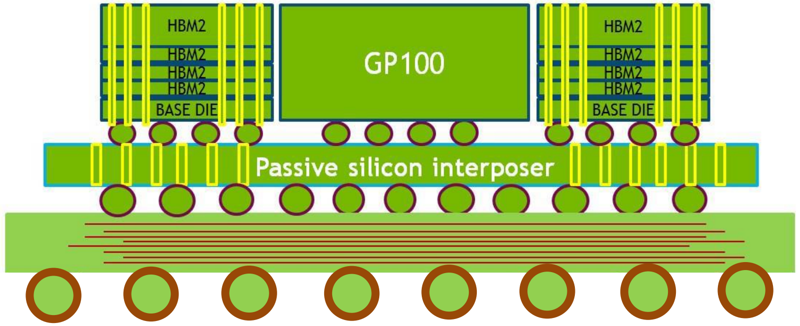


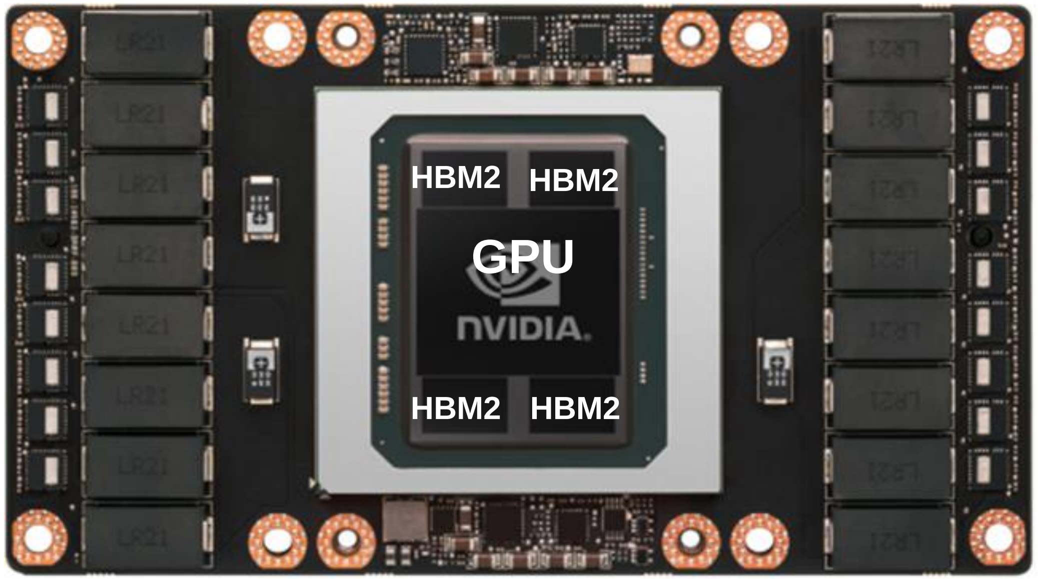
TSV-Interposer

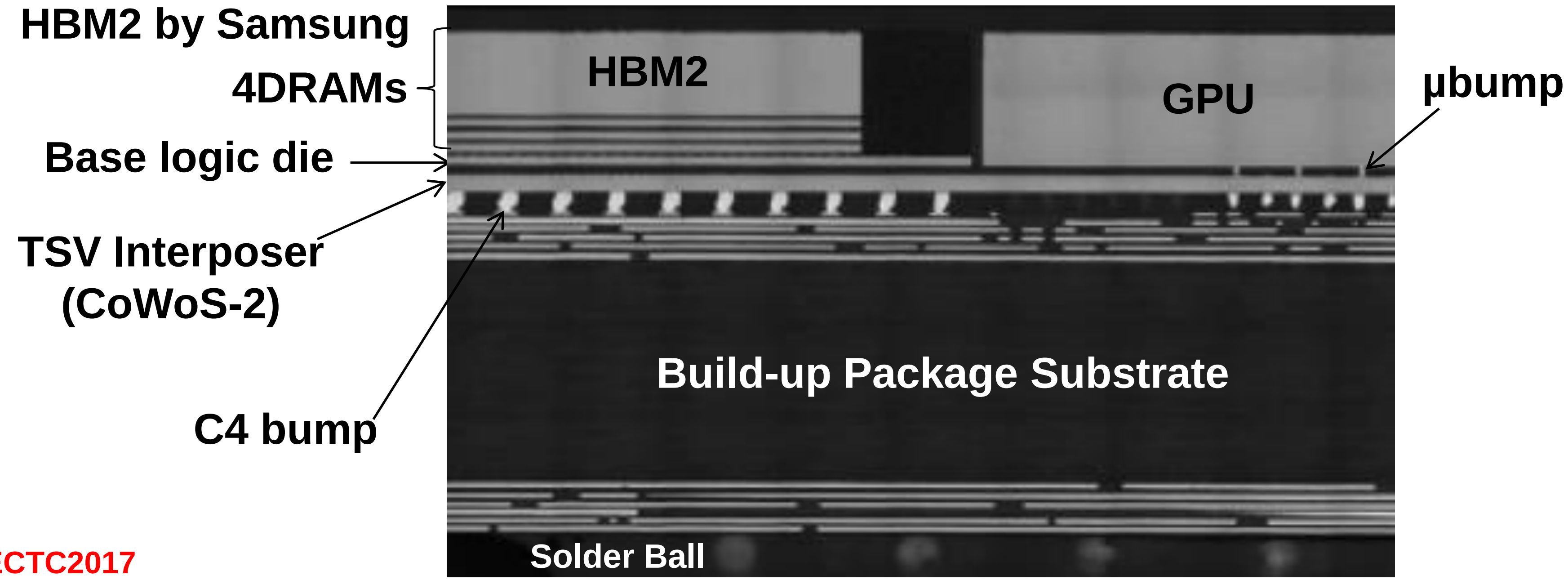
Build-up organic substrate

PDC, ECTC2016

NVidia's P100 with TSMC's CoWoS-2 and Samsung's HBM2



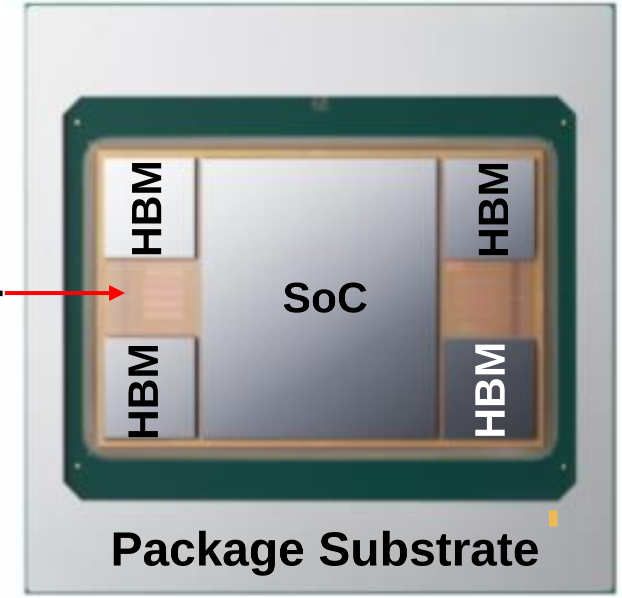




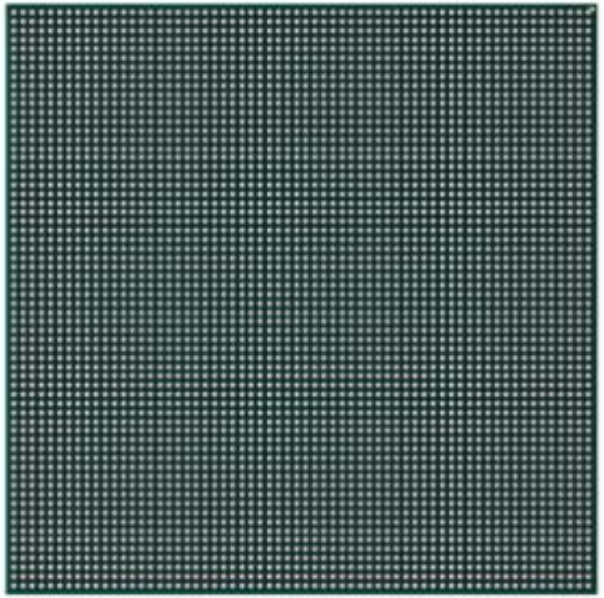
PDC, ECTC2017

Samsung's Interposer-Cube4 (I-Cube4) (2.5D IC Integration)

TSV
Interposer

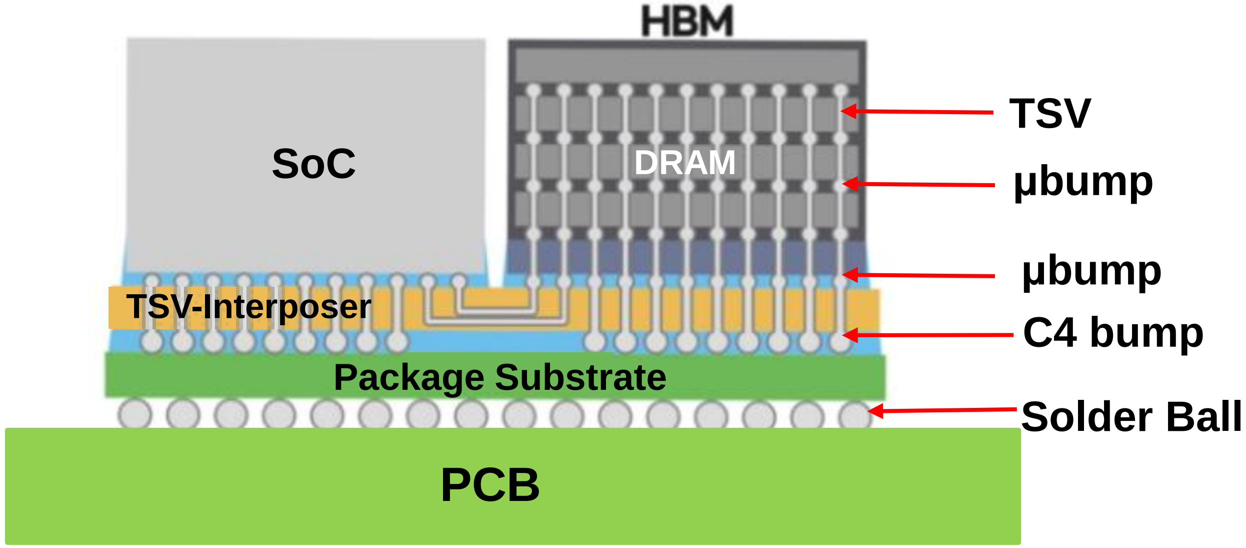


Top View



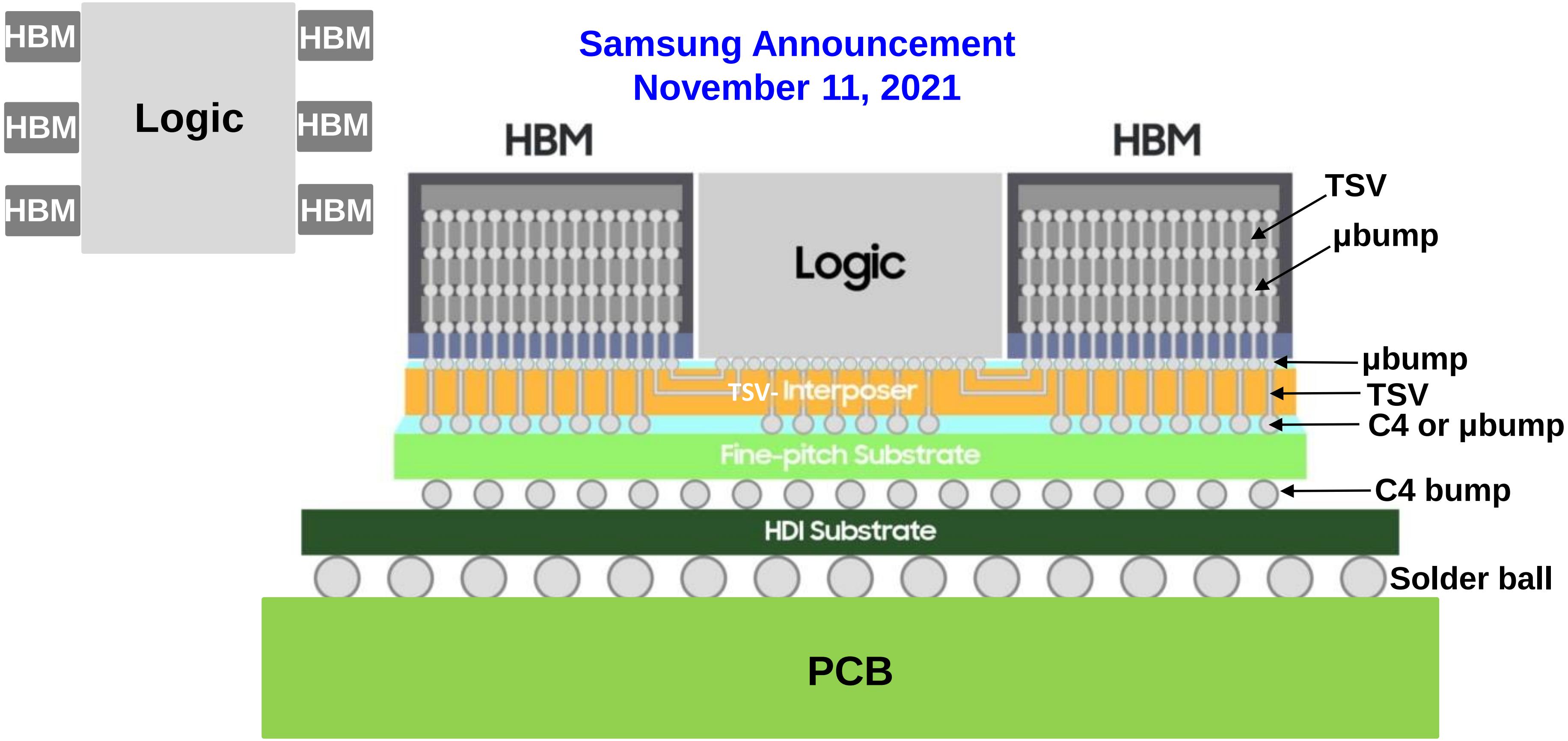
Bottom View

Cross-section
View



2.5D Integration Hybrid Substrate Cube (H-Cube) Solution for High Performance Applications

Samsung Announcement
November 11, 2021



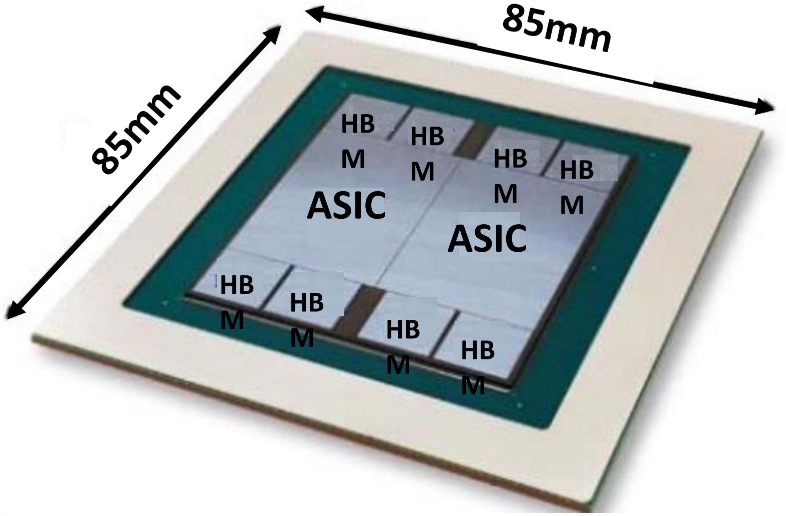
H-Cube Concept

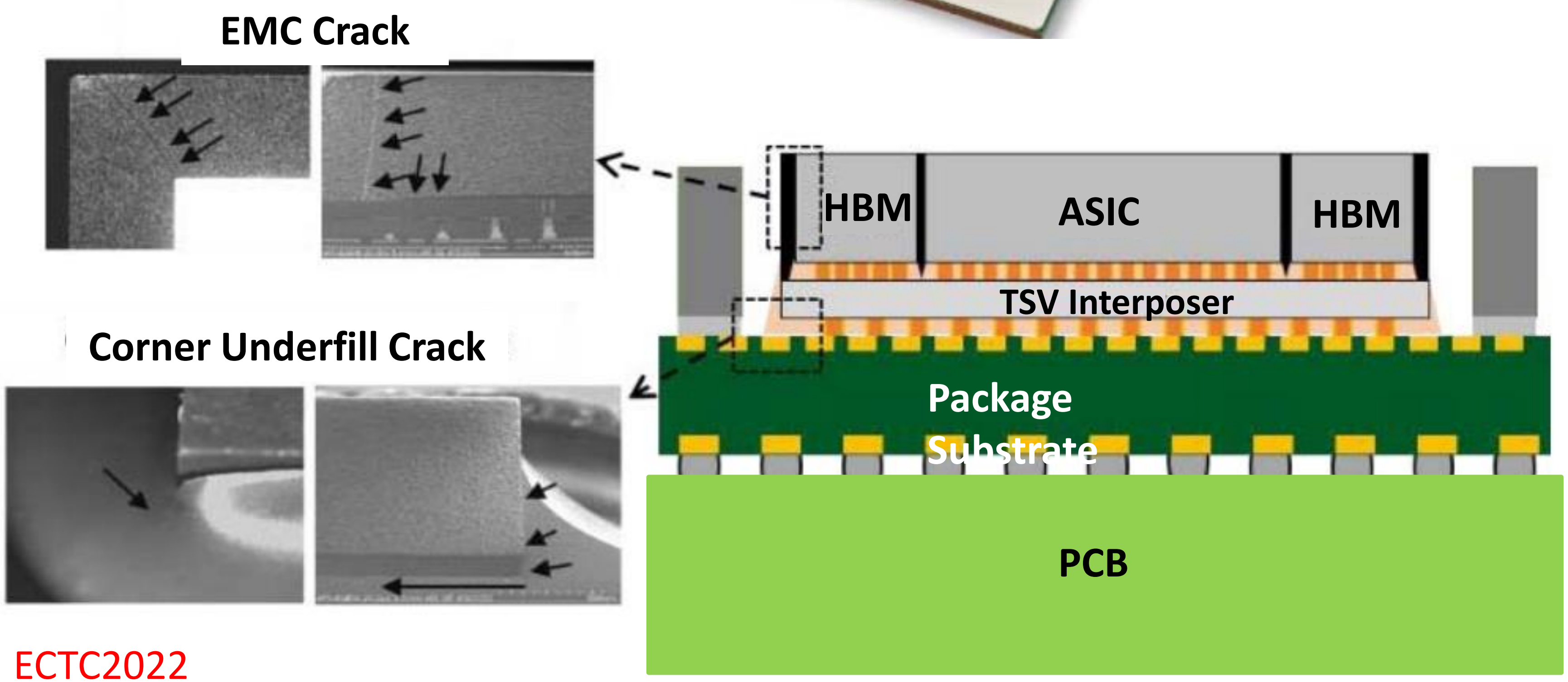
When integrating six or more HBMs, the difficulty in manufacturing the large-area substrate increases rapidly, resulting in decreased efficiency. Samsung solved this problem by applying a hybrid substrate structure in which HDI substrates that are easy to implement in large-area are overlapped under a high-end fine-pitch substrate. By decreasing the pitch of solder ball, which electrically connects the chip and the substrate, by 35% compared to the conventional ball pitch, the size of fine-pitch substrate can be minimized, while adding HDI substrate (module PCB) under the fine-pitch substrate to secure connectivity with the system board.

November 2021

Multiple system and heterogeneous integration (Samsung's MIoS)

(a)

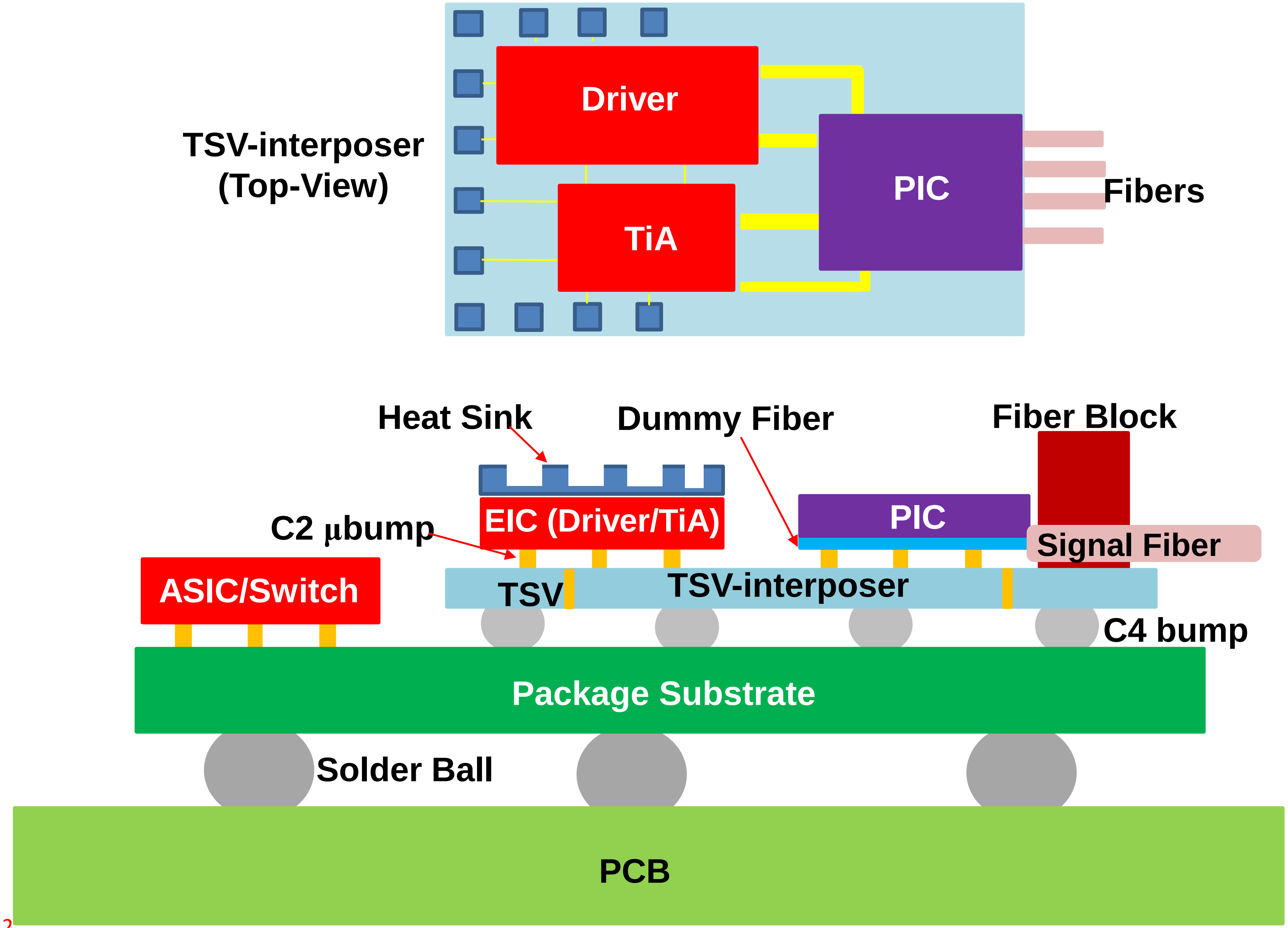




ECTC2022

(b)

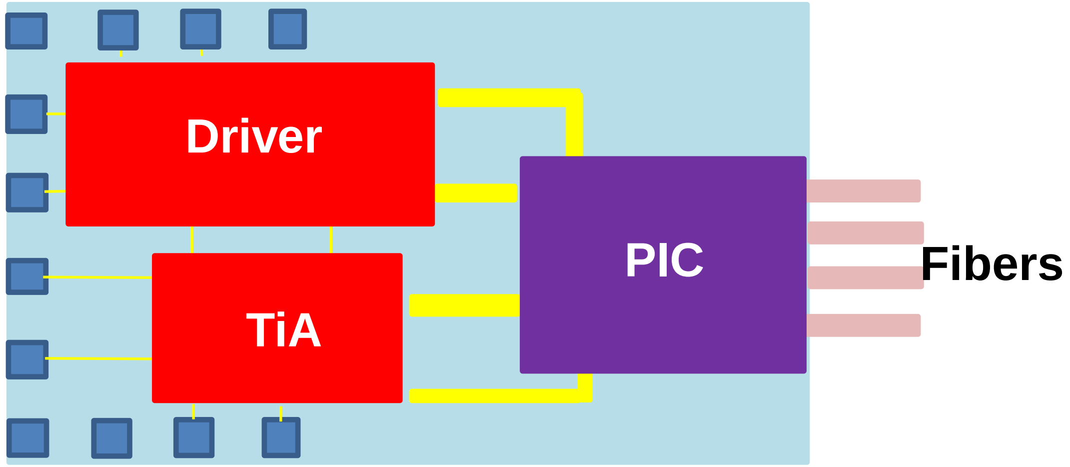
Heterogeneous Integration of PIC and EIC Devices (Co-Packaged Optic)

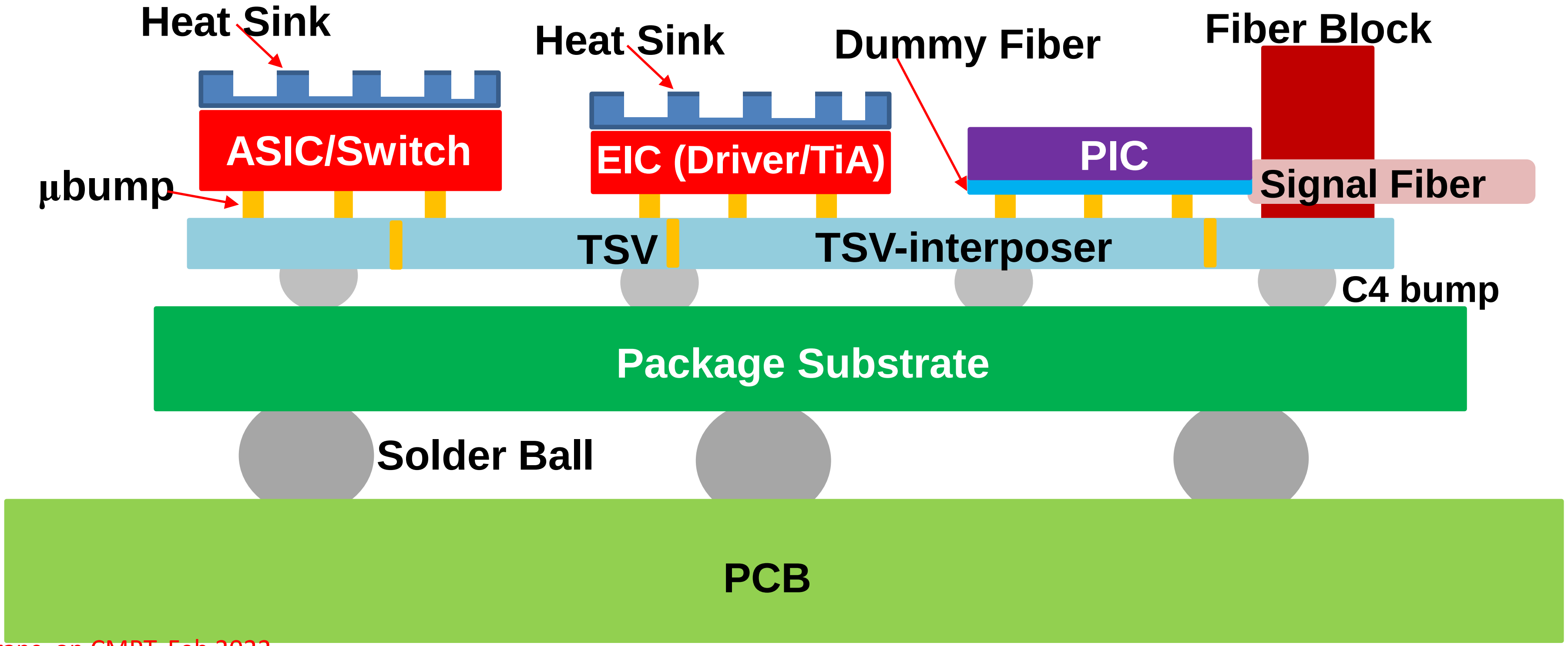


IEEE Trans. on CMPT, Feb 2022

Heterogeneous Integration of PIC and EIC Devices

EIC and PIC integration
(Top-View)



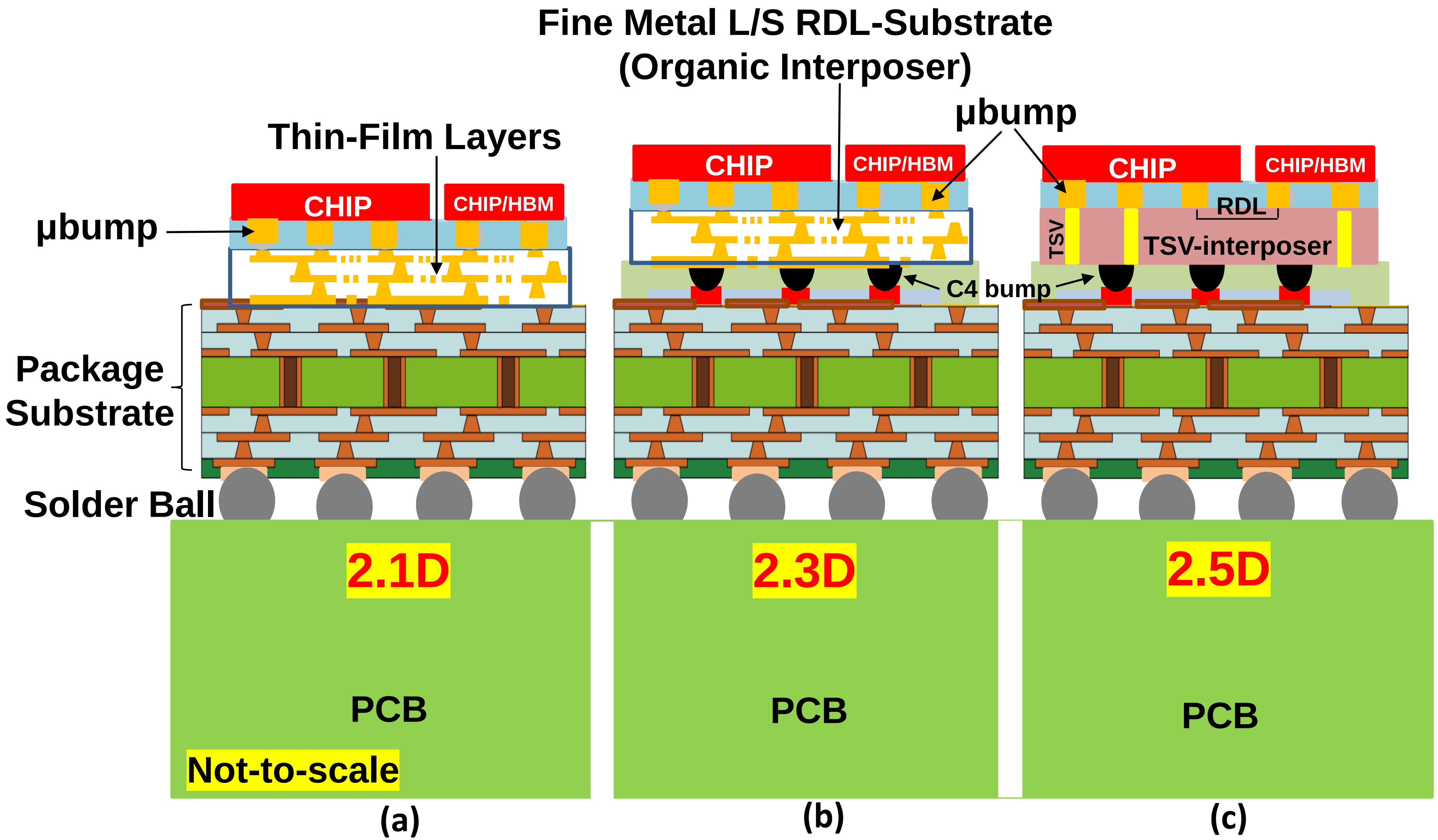


IEEE Trans. on CMPT, Feb 2022

2.3D IC Integration

- Chip-First (either face-up or face-down)
- Chip-Last (RDL-First)

2.1D, 2.3D, and 2.5D IC Integration

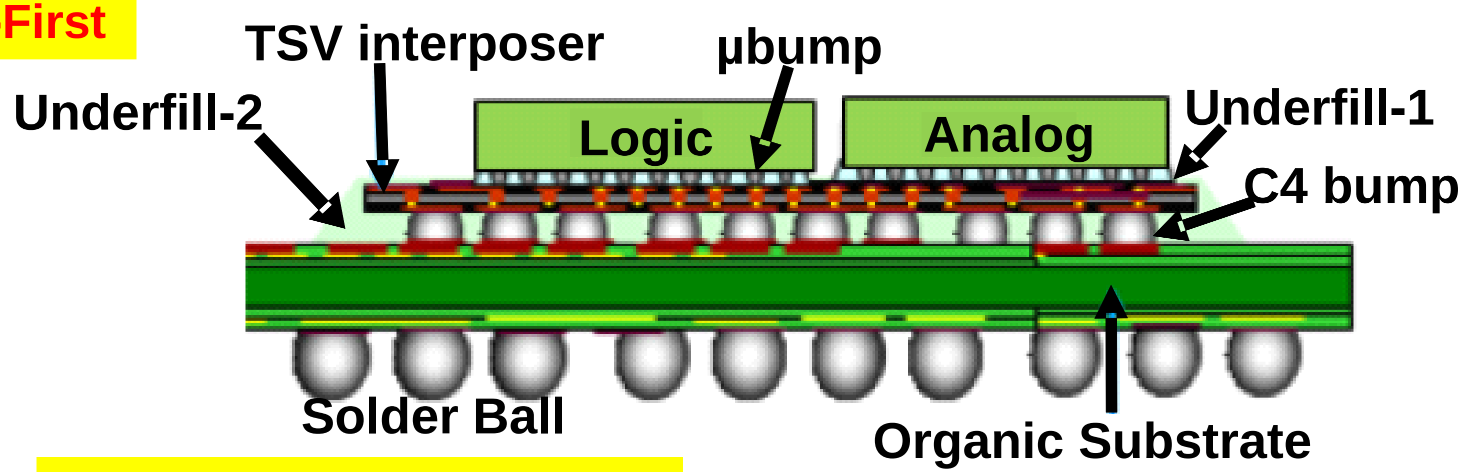


Thin-Film Layers = Fine Metal L/S RDL-Substrate (Organic Interposer)

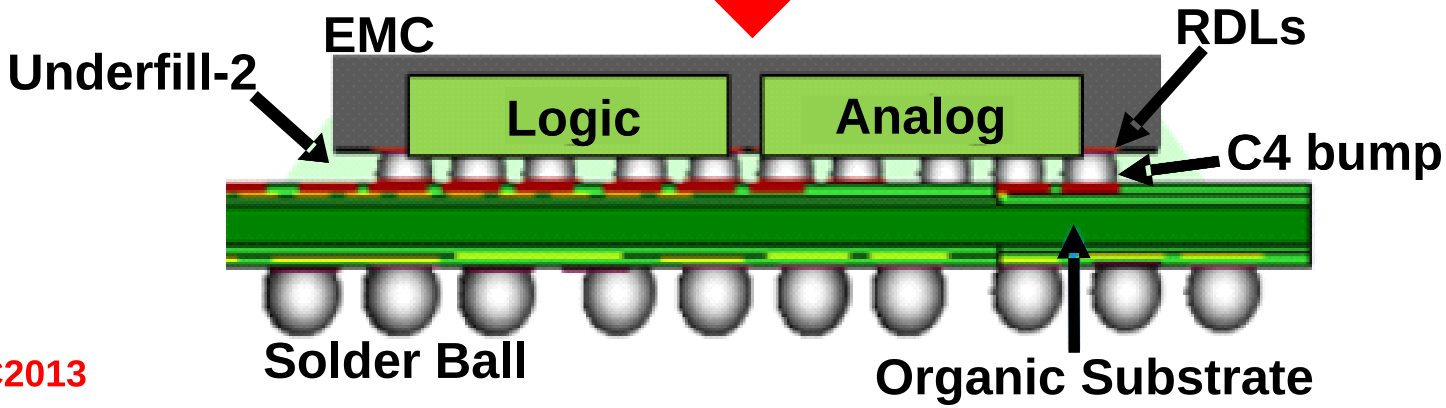
Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions

Seung Wook Yoon, Patrick Tang, Roger Emigh, Yaojian Lin, Pandi C. Marimuthu, and Raj Pendse
STATSChipPAC Ltd., 5 Yishun Street 23, Singapore 768442

Chip-First



- **The µbump, underfill-1, and TSV-interposer are eliminated.**
- **The RDLs are made by fan-out technology.**



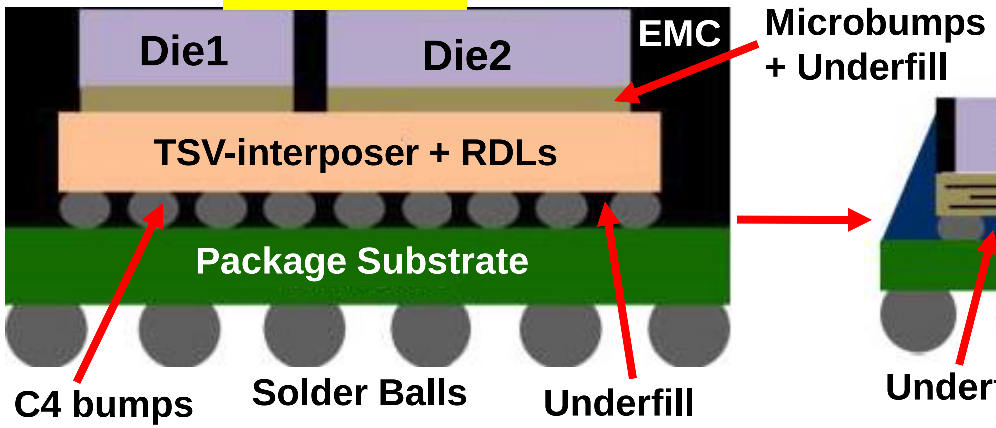
IEEE/ECTC2013

Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate (FOCoS)

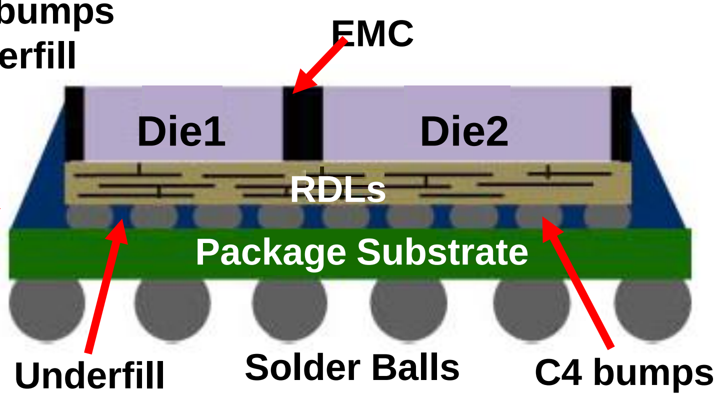
Yuan-Ting Lin, Wei-Hong Lai, Chin-Li Kao, Jian-Wen Lou, Ping-Feng Yang, Chi-Yu Wang, and Chueh-An Hseih*
Advanced Semiconductor Engineering (ASE), Inc.
e-mail: Adren_Hsieh@aseglobal.com

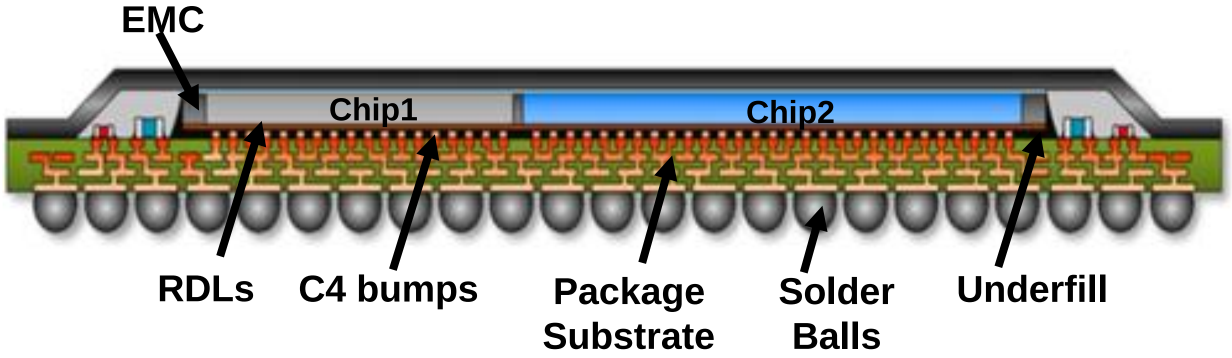
Chip-First

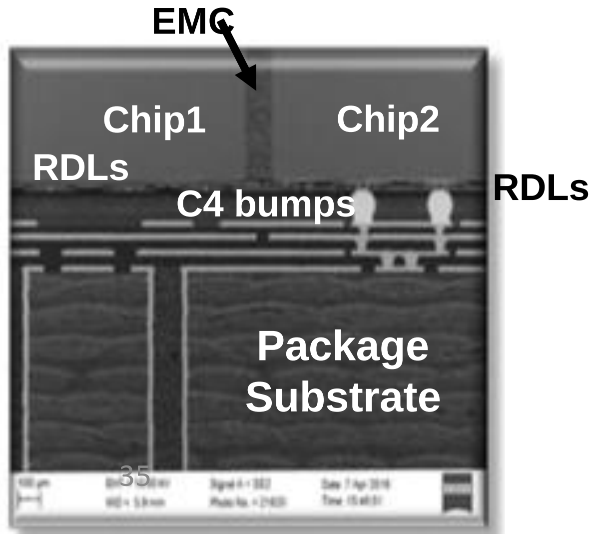
CoWoS



ASE's FOCoS





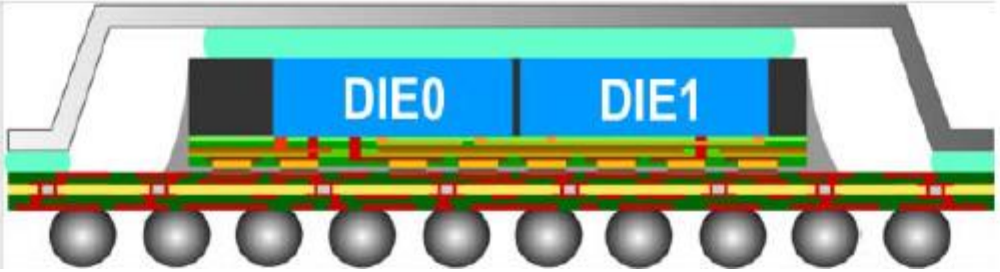


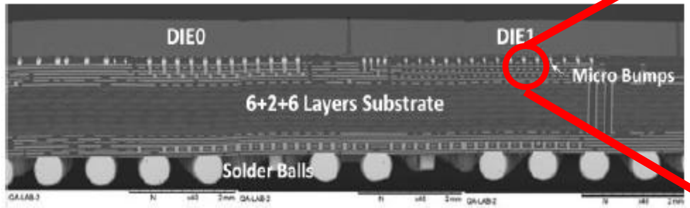
IEEE/ECTC2016

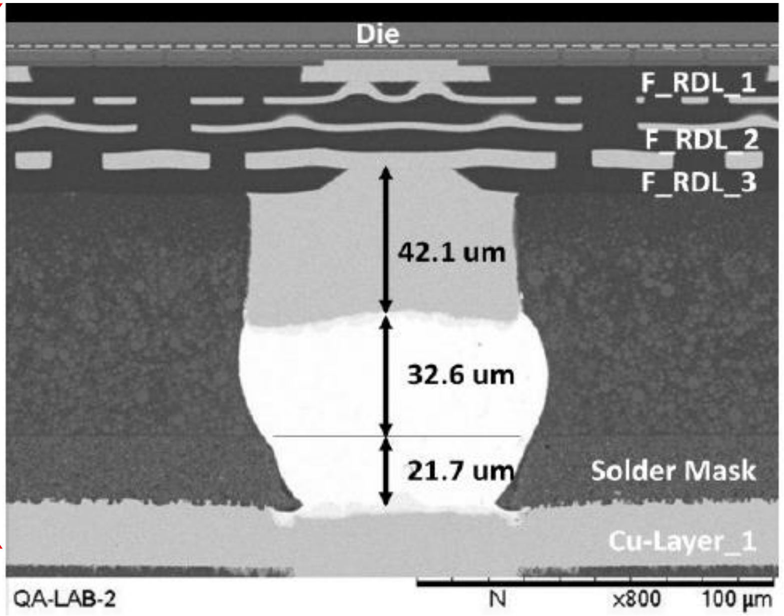
A Novel System in Package with Fan-out WLP for high speed SERDES application

Nan-Cheng Chen, Tung-Hsien Hsieh, Jimmy Jinn, Po-Hao Chang, Fandy Huang, JW Xiao, Alan Chou, Benson Lin
Mediatek Inc Hsin-Chu City, Taiwan

Chip-First



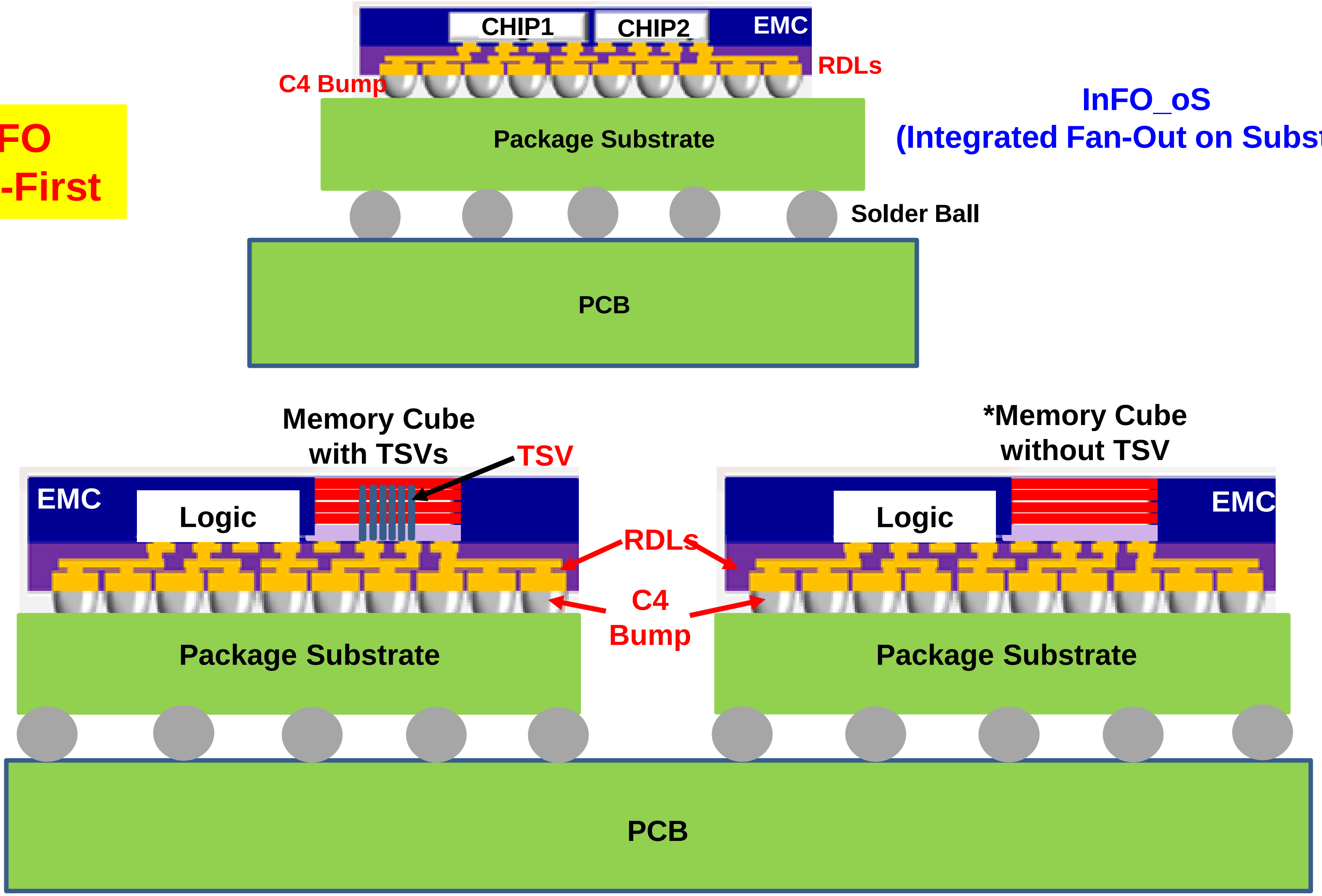




IEEE/ECTC2016

TSMC's InFO_oS and InFO_MS for Heterogeneous Integrations

InFO
Chip-First



InFO_oS
(Integrated Fan-Out on Substrate)

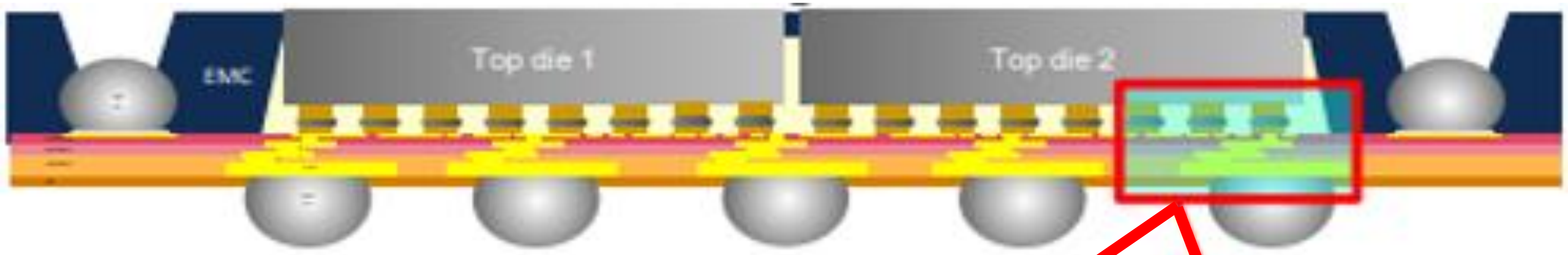
InFO_MS (Integrated Fan-Out with Memory on Substrate)

SEMICON Taiwan, September 2018, Mar 2019

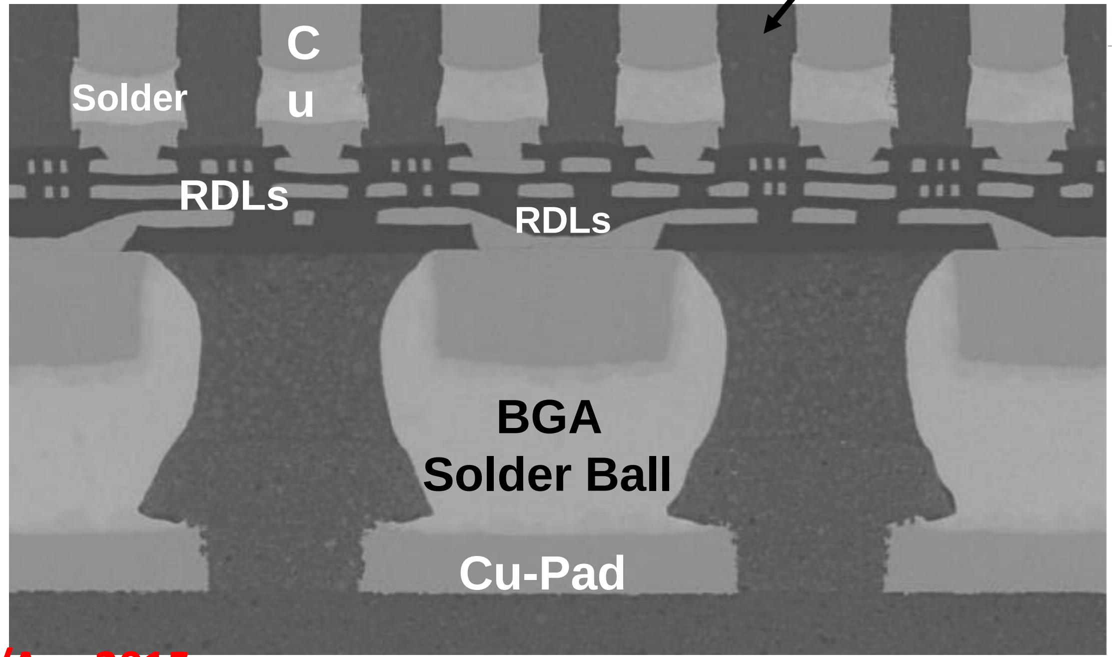
SWIFT (Silicon Wafer Integrated Fan-out Technology) Package Technology

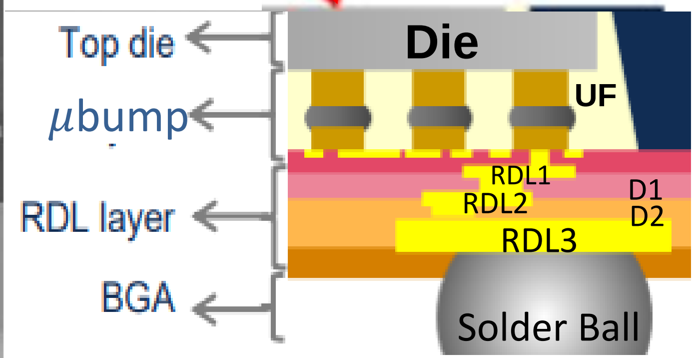
Ron Huemoeller and C. Zweng
Amkor Technology
Tempe, AZ 85284

Chip-Last



Underfill (UD)





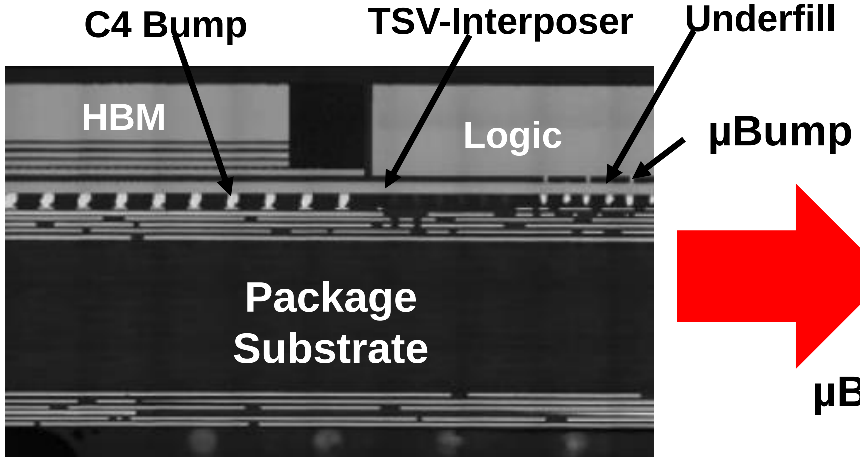
Chip Scale Review, Mar/Apr 2015

Low Cost Si-less RDL Interposer Package for High Performance Computing Applications

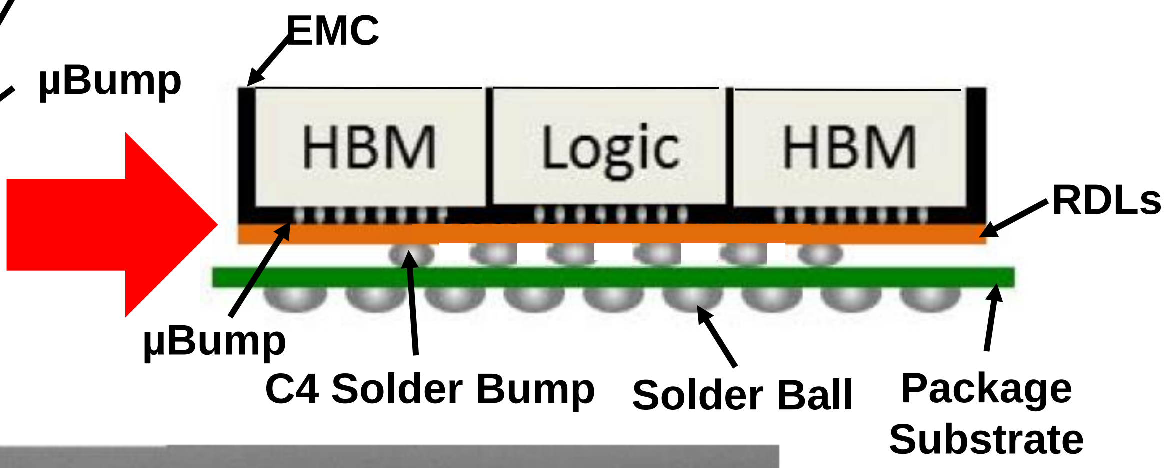
Kyoung-Lim Suk*, Seok Hyun Lee, Jong Youn Kim, Seok Won Lee, Hak Jin Kim, Su Chang Lee, Pyung Wan Kim, Dae-Woo Kim, and Dan (Kyung Suk) Oh
Package Development Team, Samsung Electronics Co., Ltd.
Gyeonggi-do, Republic of Korea
***klim.suk@samsung.com**

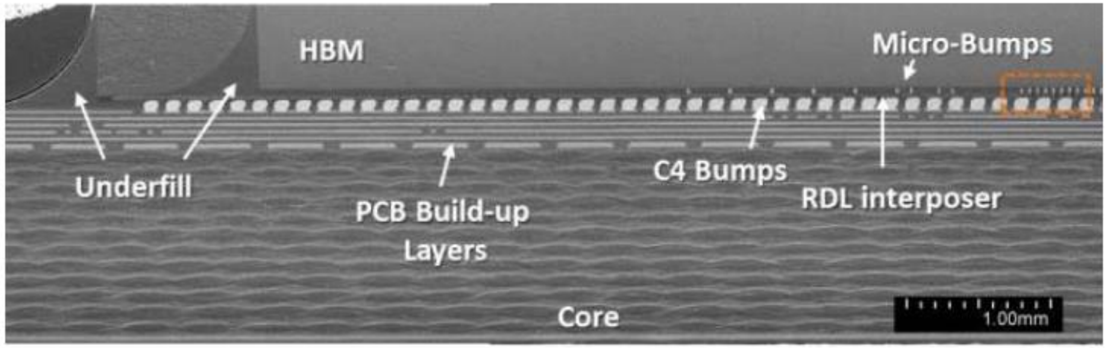
Chip-Last

CoWoS



Si-less RDL-Interposer





IEEE/ECTC2018

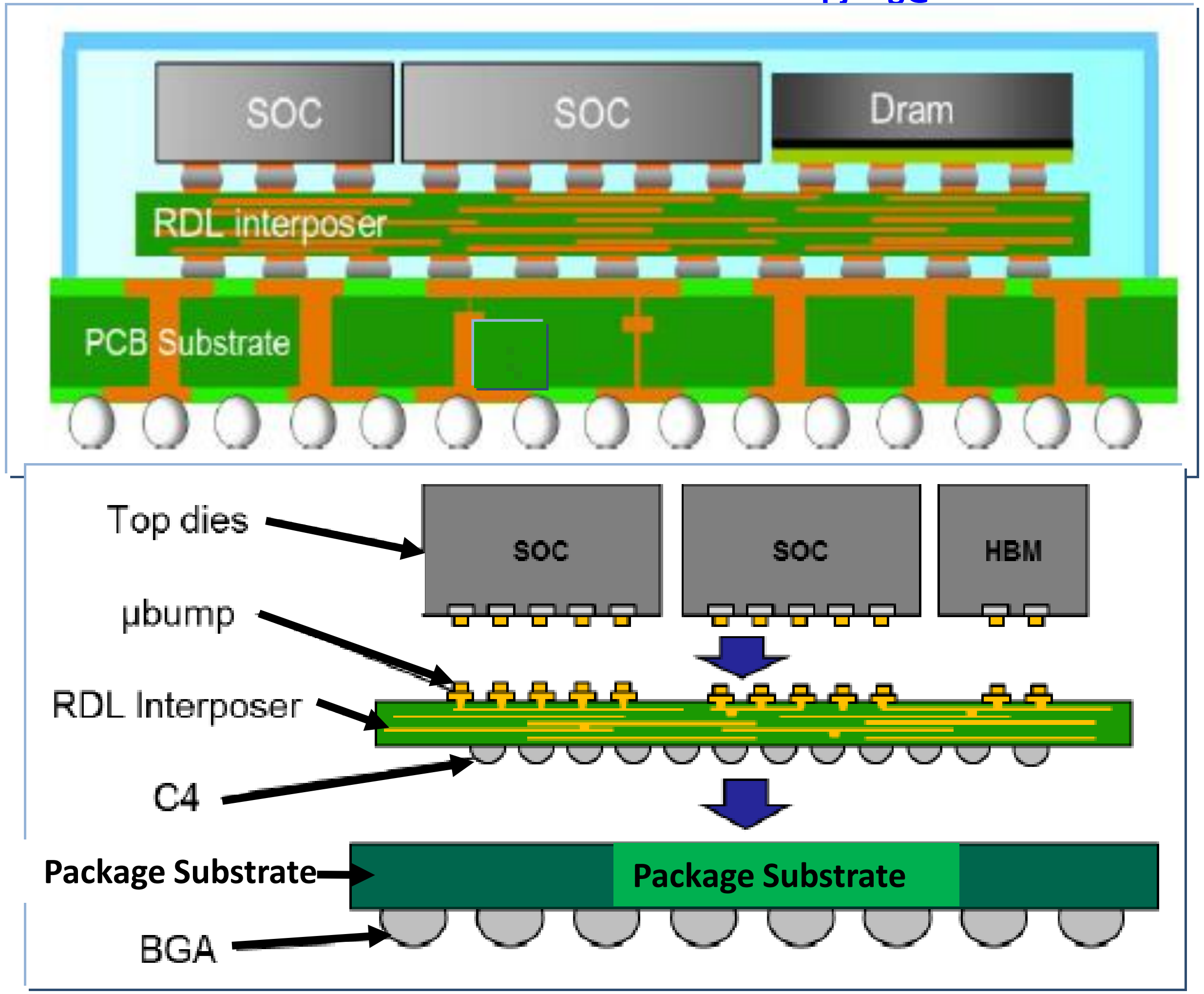
Heterogeneous Integration with Multilayer RDL Interposer

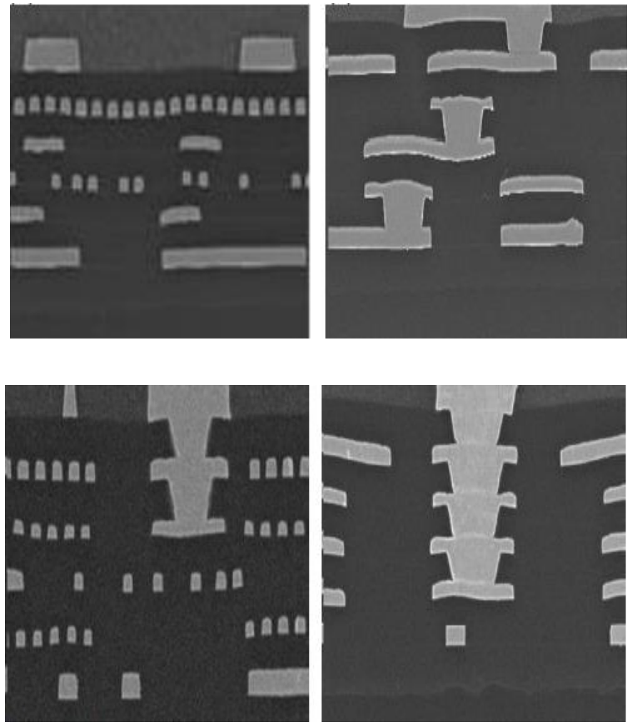
Yi-Hang Lin, M.C.Yew, M.S. Liu ,S.M. Chen, T.M. Lai, P.N. Kavle, C.H. Lin, T.J. Fang, C.S. Chen, C.T. Yu, K.C. Lee, C.K. Hsu, P.Y. Lin, F.C Hsu and Shin-Puu Jeng*

TSMC, No.6, Creation Rd. II, Hsinchu Science Park, Hsinchu, Taiwan (R.O.C.) 30077

Email: *spjeng@tsmc.com

Chip-Last



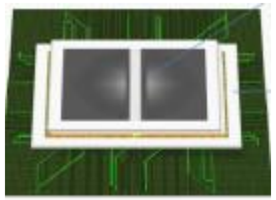


ECTC2019

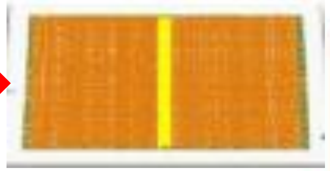
Ultra High Density IO Fan-Out Design Optimization with Signal Integrity and Power Integrity

Keng Tuan Chang, Chih-Yi Huang, Hung-Chun Kuo, Ming-Fong Jhong, Tsun-Lung Hsieh, Mi-Chun Hung, Chen-Chao Wang
Integrated Design, Corporation Design Division, Corporate Research and Development,
Advanced Semiconductor Engineering (ASE), Inc.,
No. 26, Chin 3rd Road Nantze Export Processing Kaohsiung 811, Taiwan
Email: gordon_chang@aseglobal.com

Chip-Last

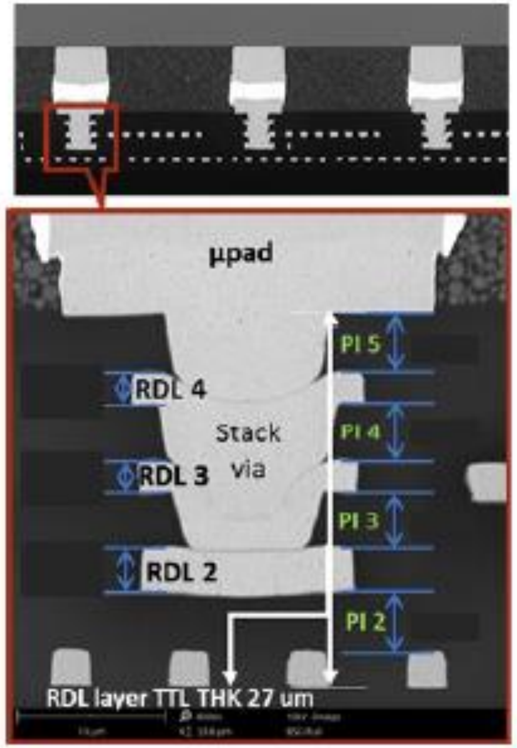


CoWoS

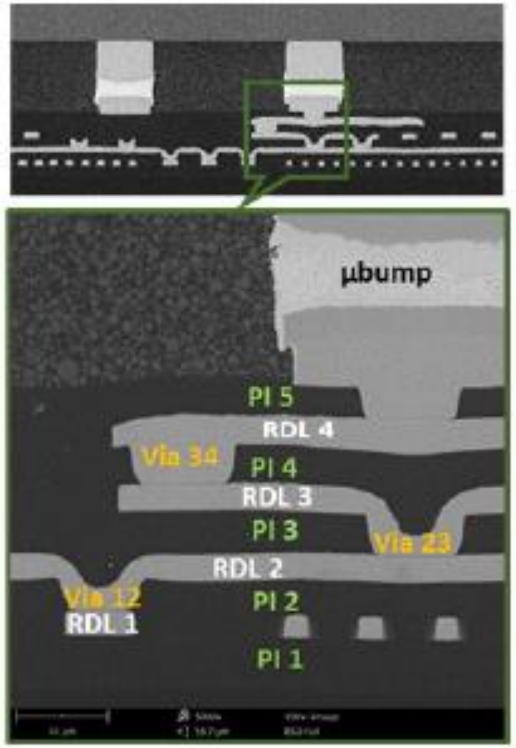


FOCoS

Stacked Vias



Non-stacked Vias



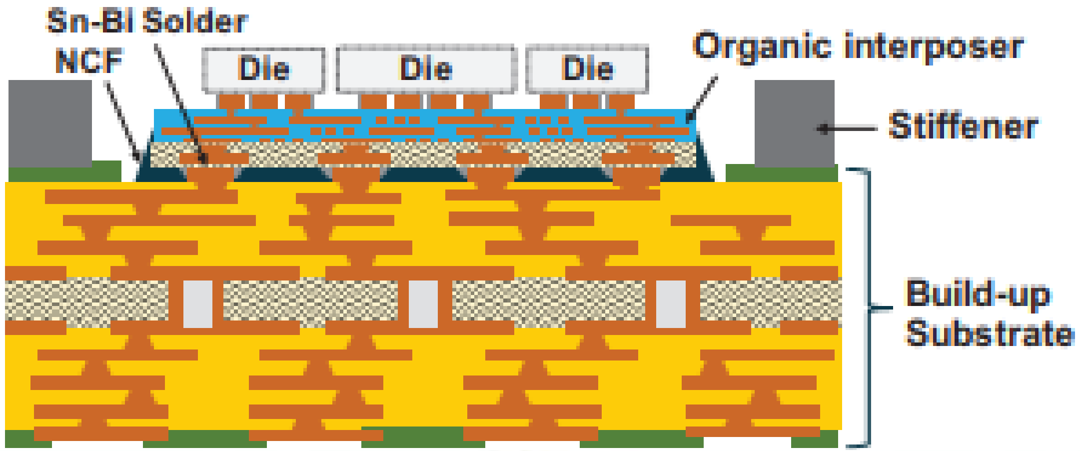
Cross sections of FOCoS

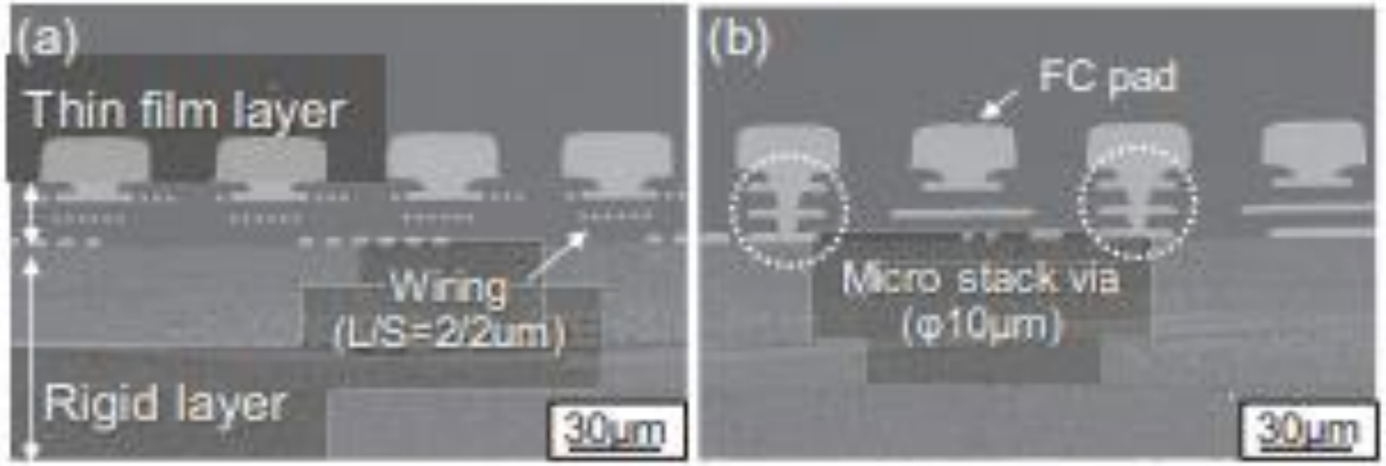
ECTC2019

Development of 2.3D High Density Organic Package using Low Temperature Bonding Process with Sn-Bi Solder

Shota Miki, Hiroshi Taneda, Naoki Kobayashi, Kiyoshi Oi, Koji Nagai, Toshinori Koyama Process Development Dept. Research & Development Div. SHINKO ELECTRIC INDUSTRIES CO., LTD. Nagano-shi, Japan Vy.miki@shinko.co.jp

Chip-Last



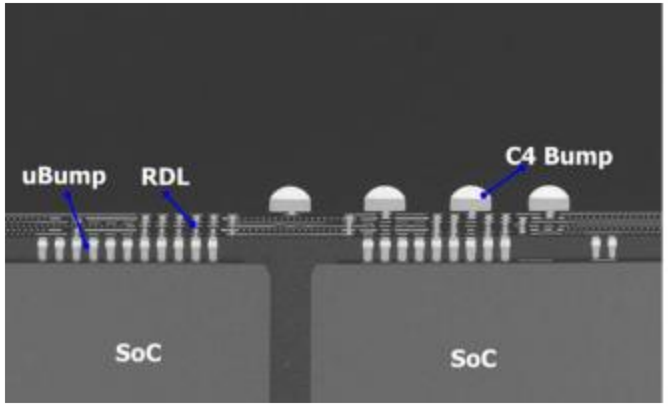


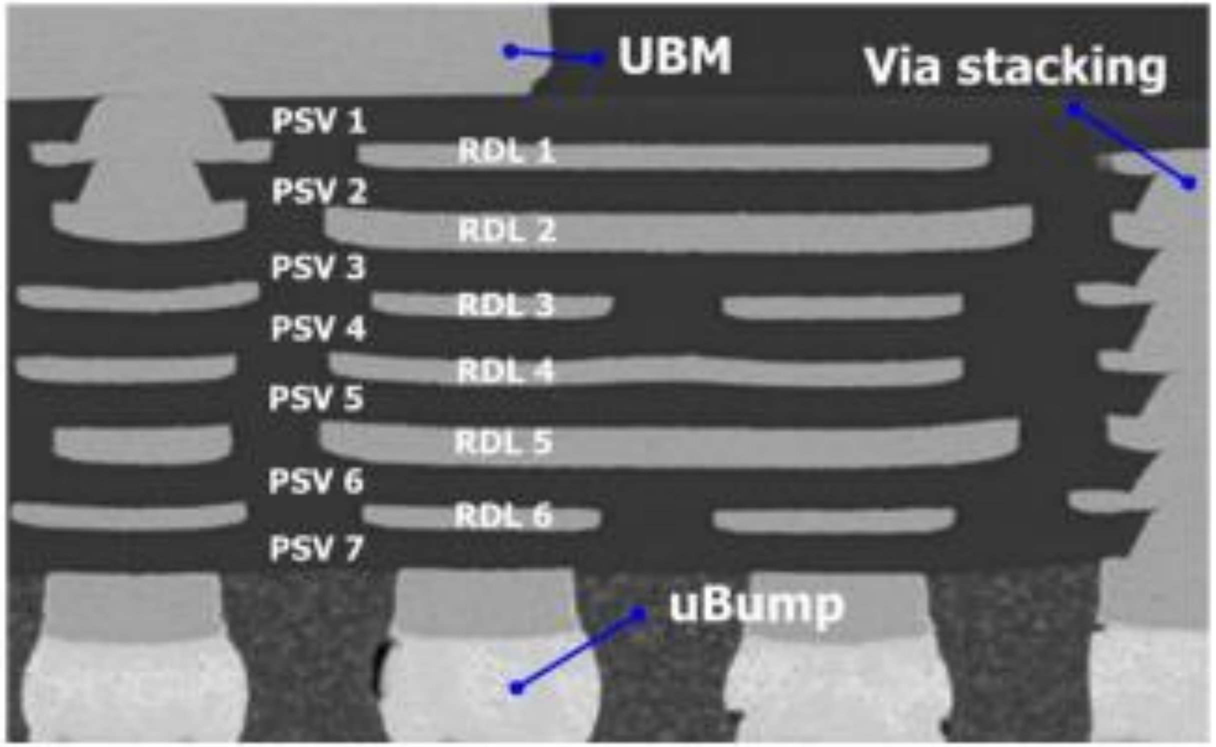
IEEE/ECTC2019, 2020

Large Size Multilayered Fan-Out RDL Packaging for Heterogeneous Integration

Jay Li*, Fang-Lin Tsai, Jackson Li, George Pan, Mu-Hsuan Chan, Louise Zheng, Steven Chen, Nicholas Kao, David Lai, Katch Wan and Yu-Po Wang, SPIL
153, Sec. 3, Chung-Shan Rd. Tantzu, Taichung 427, Taiwan, R.O.C. *Email: jayli@spil.com.tw ; Tel: 886-4-2534-1525 ext 4956

Chip-Last



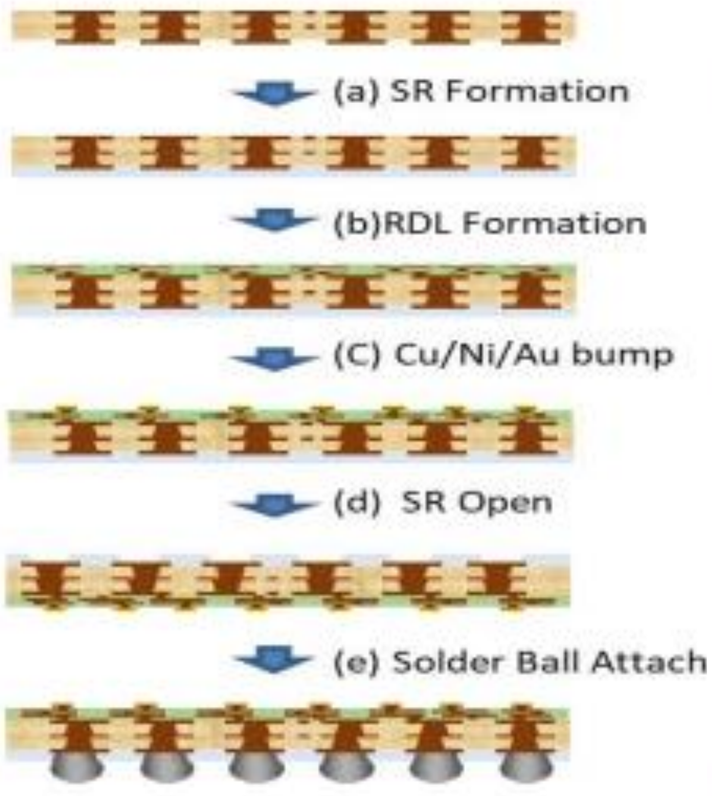


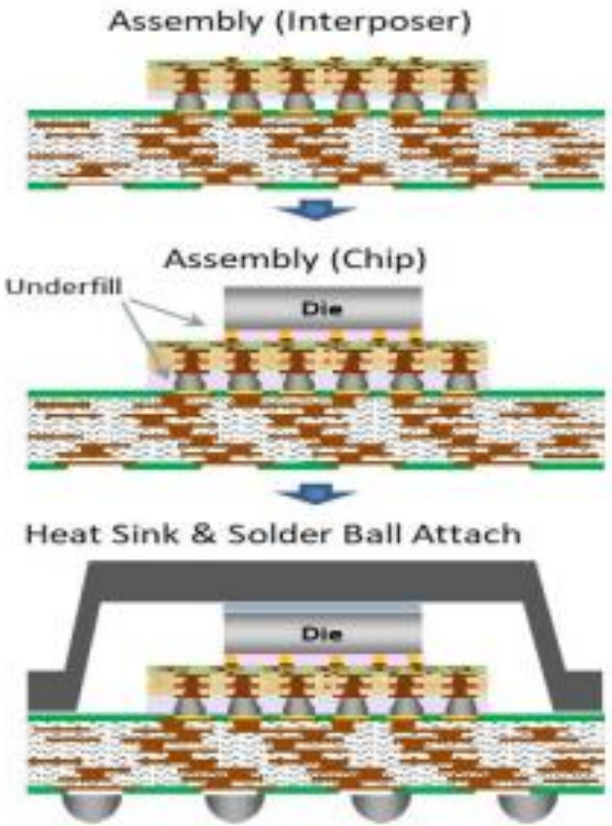
IEEE/EPTC DEC 2021

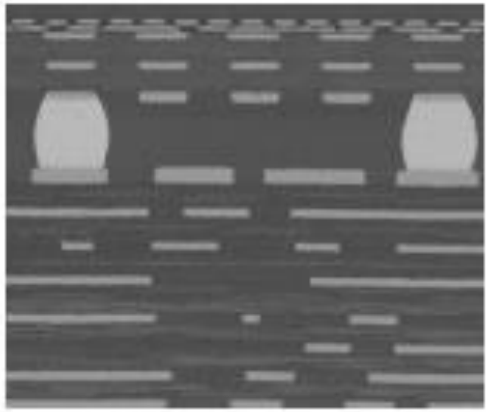
Cost Effective 2.3D Packaging Solution by using Fanout Panel Level RDL

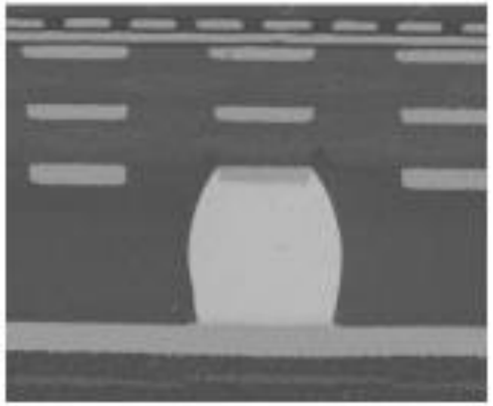
Joonsung Kim, Jaehoon Choi, Sanguk Kim, Jooyoung Choi, Yongjin Park, Gyoungbum Kim, Sangyu Kim, Sangwook Park, Hwasub Oh, Seok Won Lee, Taeje Cho and Dong Wook Kim
Test & System Package (TSP) Samsung Electronics Co., Ltd, Chonan-Si, Choongchungnam-Do, South Korea Joonsung2.kim@samsung.com

Chip-Last









IEEE/ECTC2021

Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

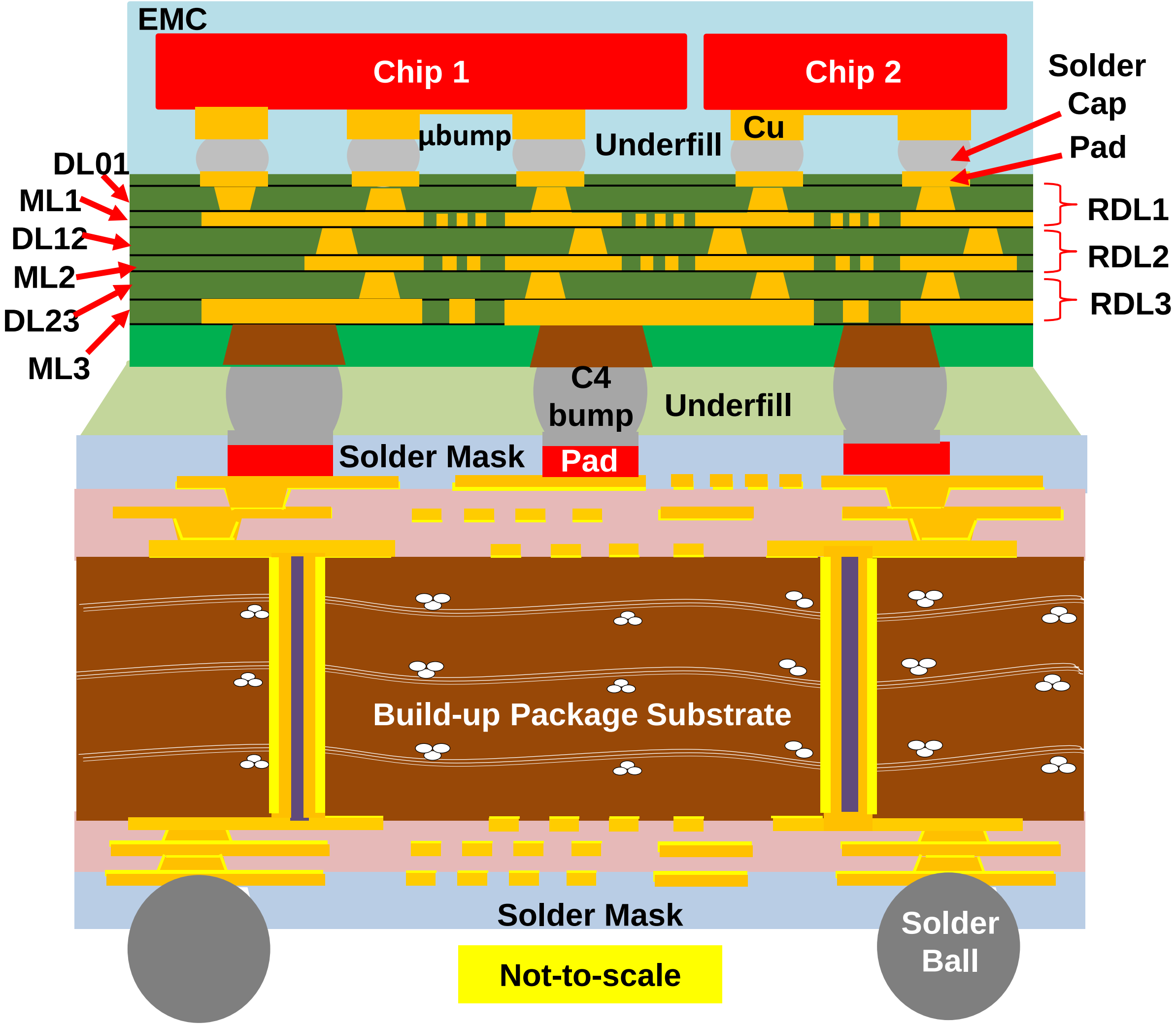
John H Lau, Gary Chang-Fu Chen, Jones Yu-Cheng Huang, Ricky Tsun-Sheng Chou, Channing Cheng-Lin Yang, Hsing-Ning Liu, and Tzvy-Jang Tseng

Unimicron Technology Corporation,

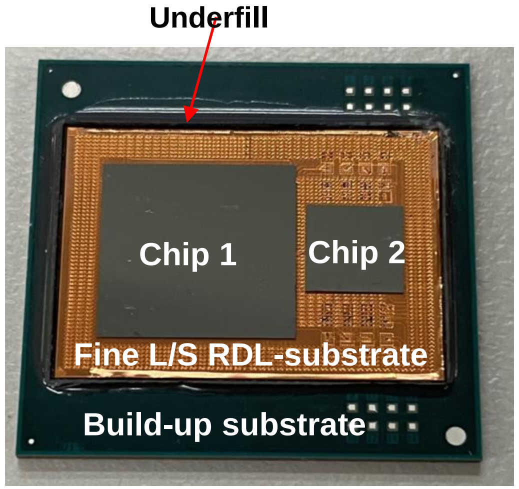
Taoyuan City, Taiwan

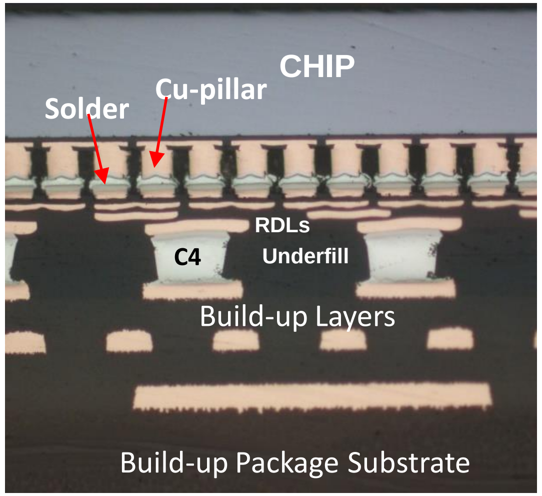
John_Lau@unimicron.com

Chip-Last



Not-to-scale





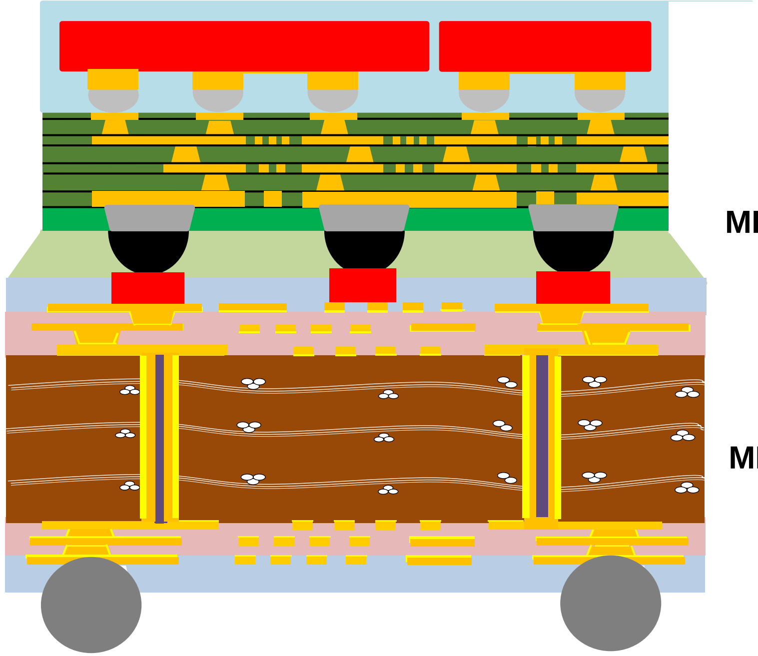
IEEE/ECTC2021

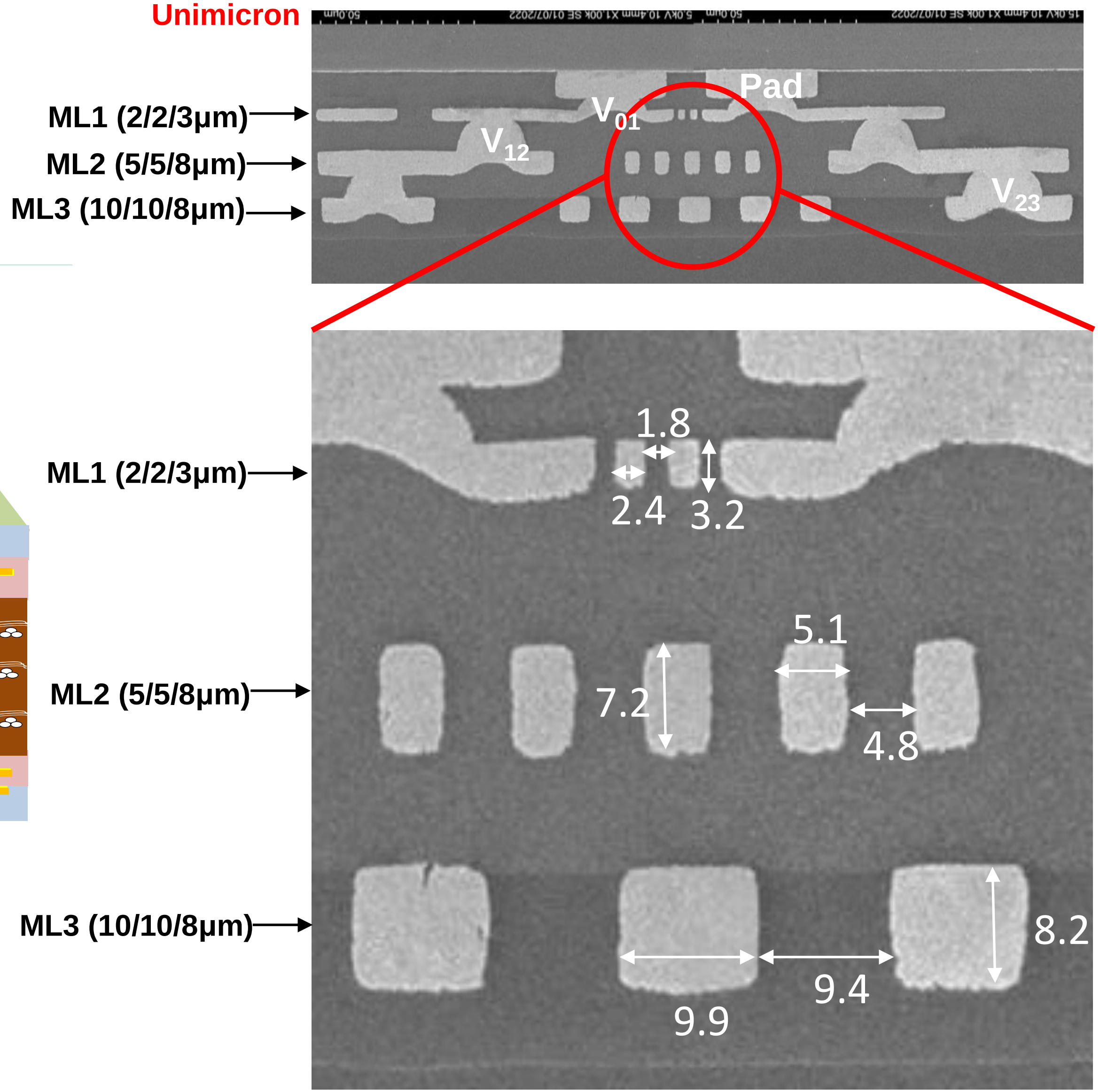
2.3D Hybrid Substrate with Ajinomoto Build-Up Film for Heterogeneous Integration

Gary Chang-Fu Chen, John H Lau, Ricky Tsun-Sheng Chou, Channing Cheng-Lin Yang, Jones Yu-Cheng Huang, Hsing-Ning Liu, and Tzyy-Jang Tseng

Unimicron

Chip-Last



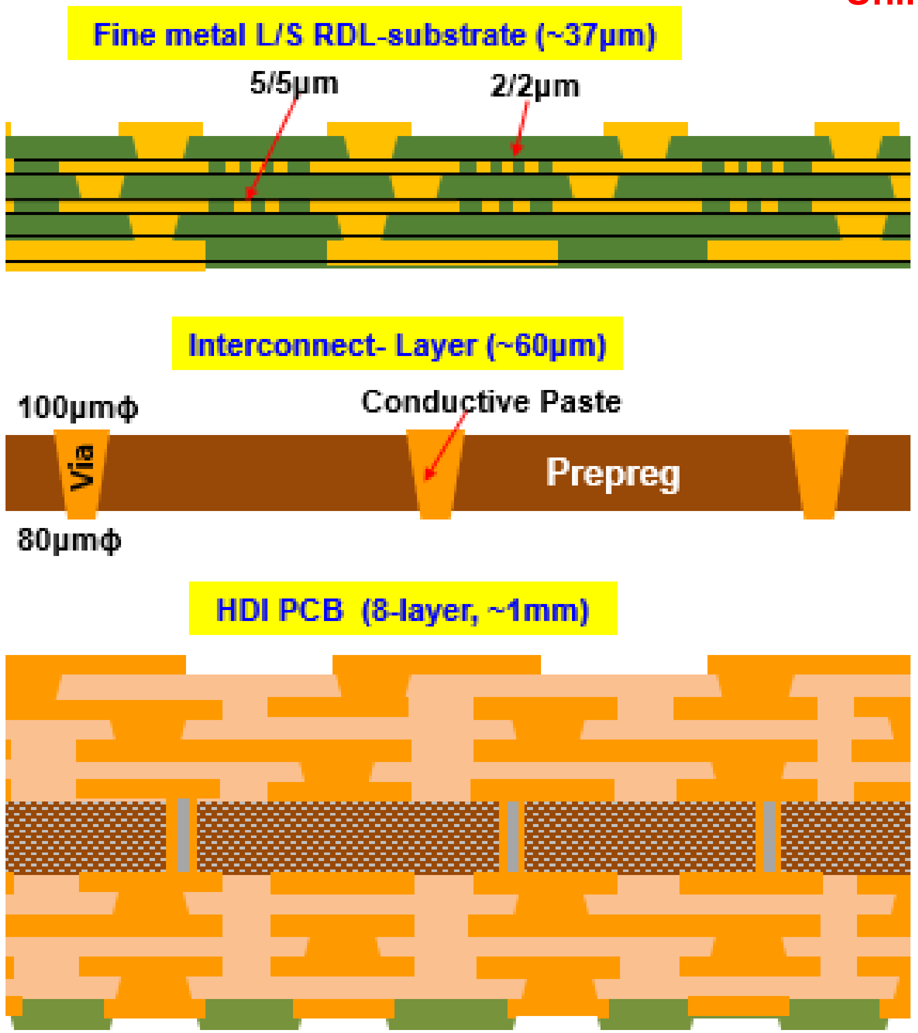


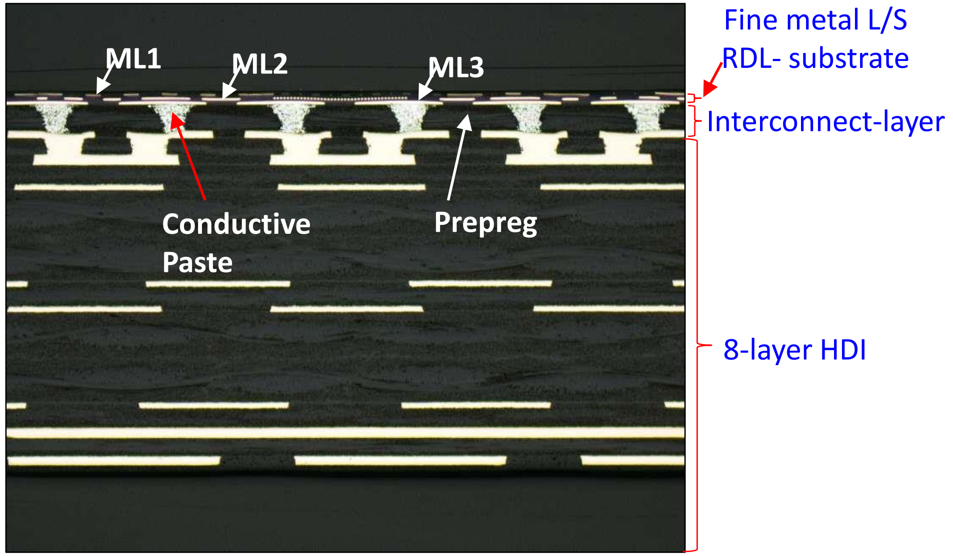
IEEE/ECTC2022

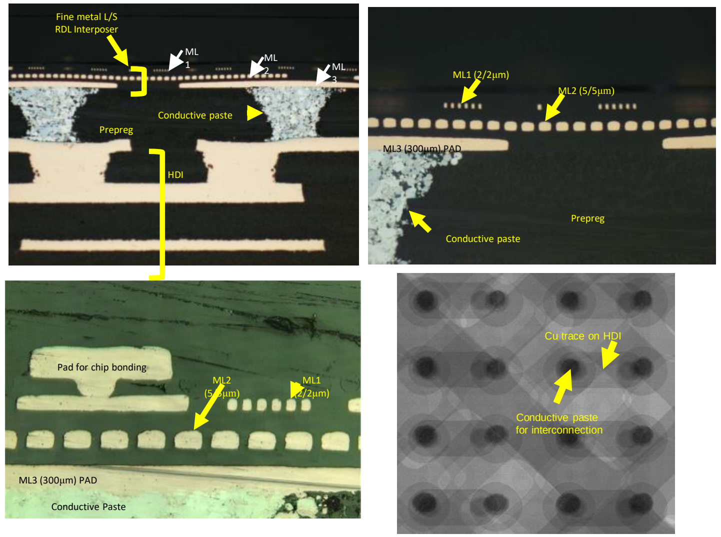
Development of High-Density Hybrid Substrate for Heterogeneous Integration

Peng, T., J. H. Lau, C. Ko, P. Lee, E. Lin, K. Yang, P. Lin, T. Xia, L. Chang, N. Liu, C. Lin, T. Lee, J. Wang, M. Ma, and T. Tseng

Unimicron





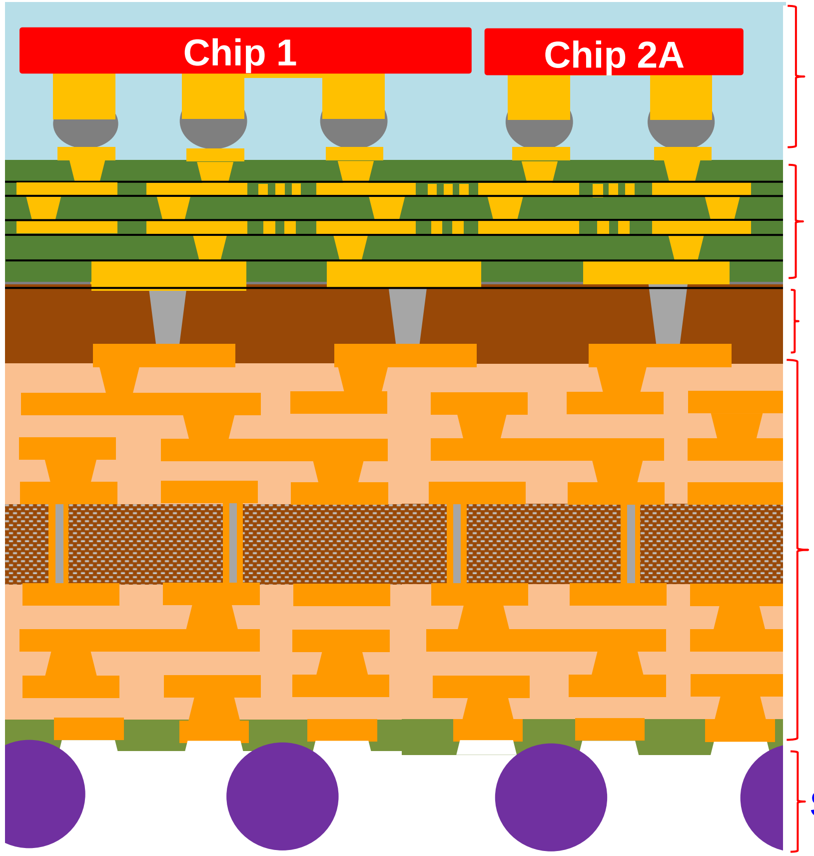


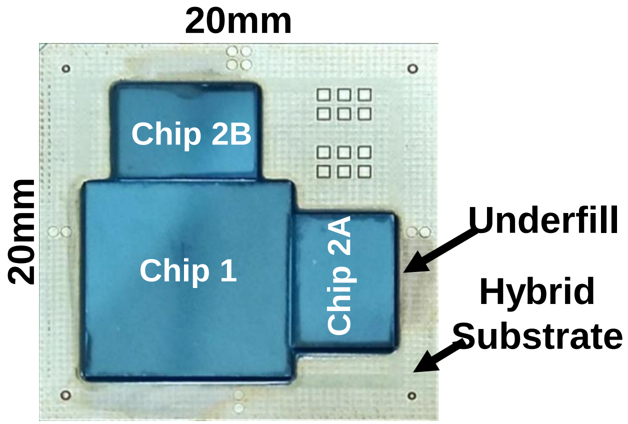
IEEE/ICSJ2021

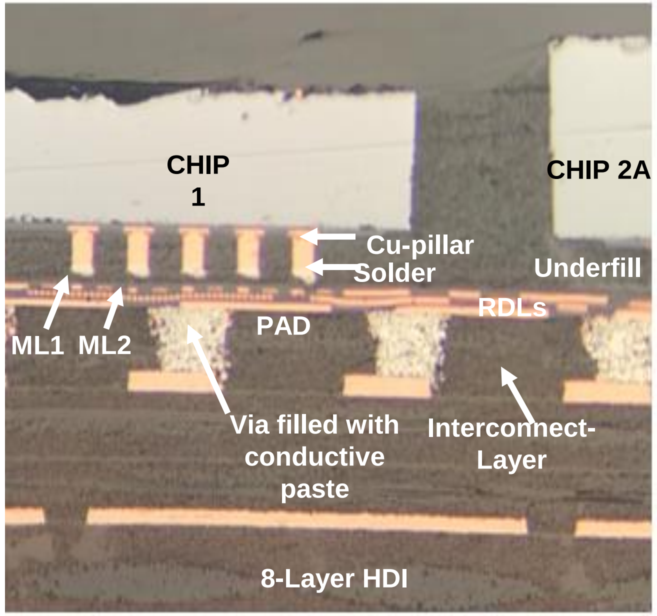
High-Density Hybrid Substrate for Heterogeneous Integration

Chia-Yu Peng , John H. Lau , Life Fellow, IEEE, Cheng-Ta Ko, Paul Lee, Eagle Lin, Kai-Ming Yang, Puru Bruce Lin, Tim Xia, Leo Chang, Ning Liu, Curry Lin, Tzu Nien Lee, Jason Wong, Mike Ma, Tzyy-Jang Tseng
Unimicron

Chip-Last







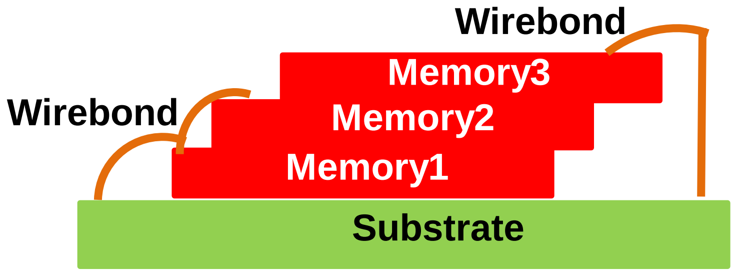
IEEE Transactions on CPMT, March 2022

3D IC Integration

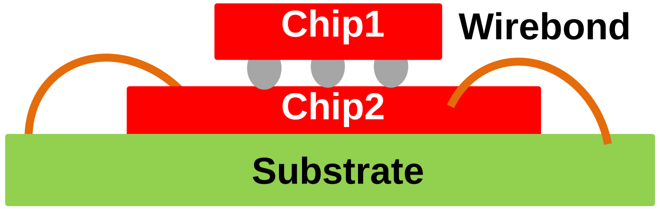
- 3D IC Packaging (without TSVs)
- 3d IC Integration (with TSVs)

3D IC Packaging (without TSVs)

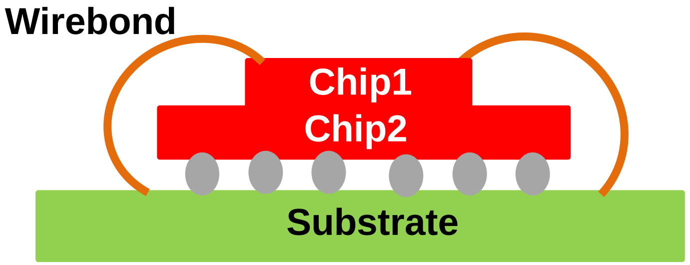
3D IC Packaging



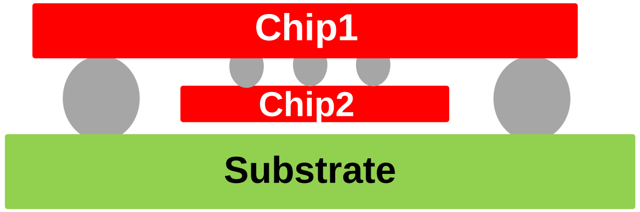
(a)



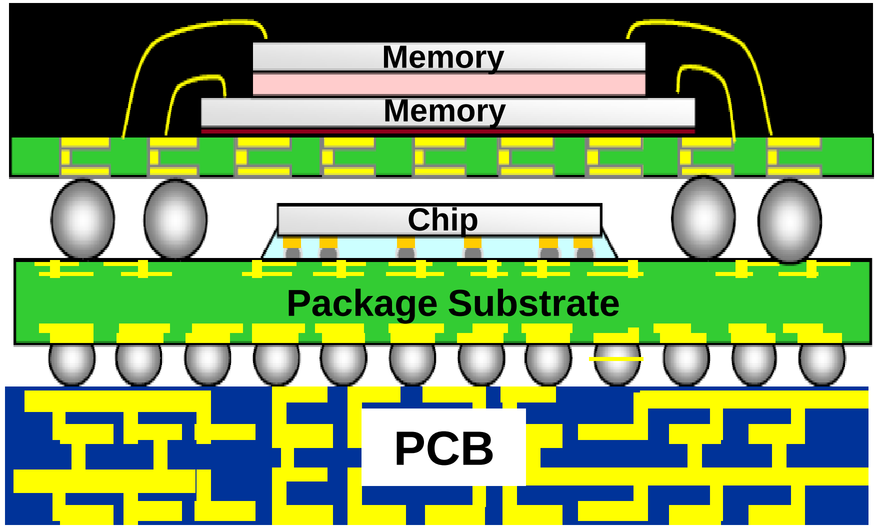
(b)



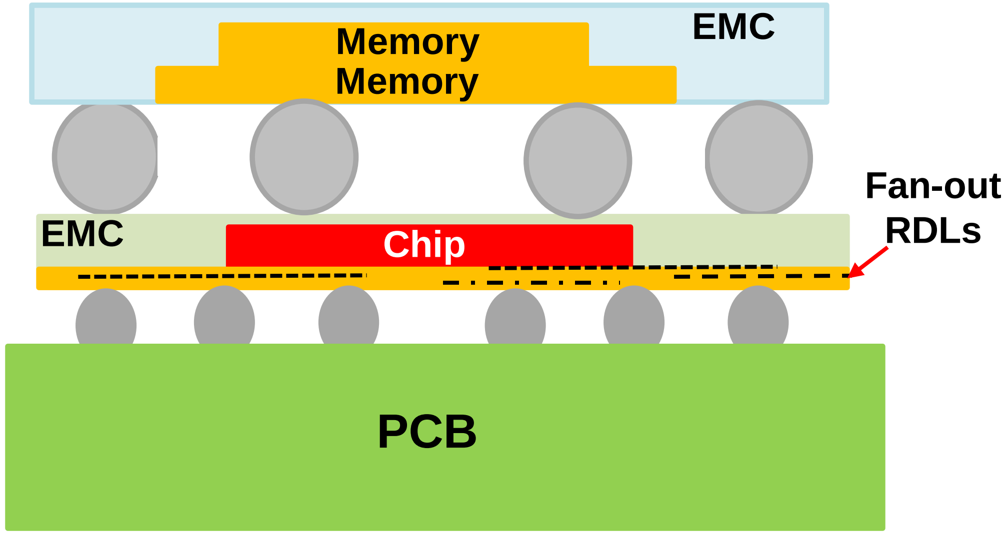
(c)



(d)



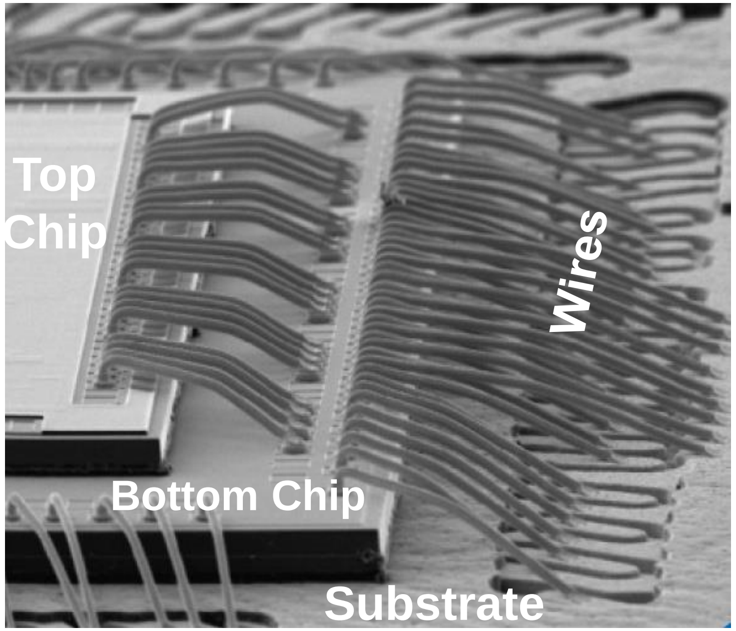
(e)

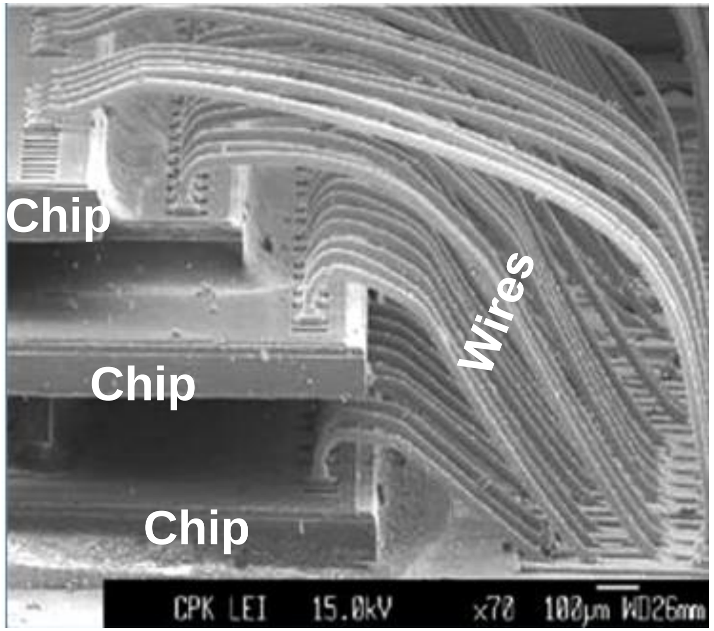


(f) Semiconductor Advanced Packaging, 2021

3D (Wirebonding) IC Packaging

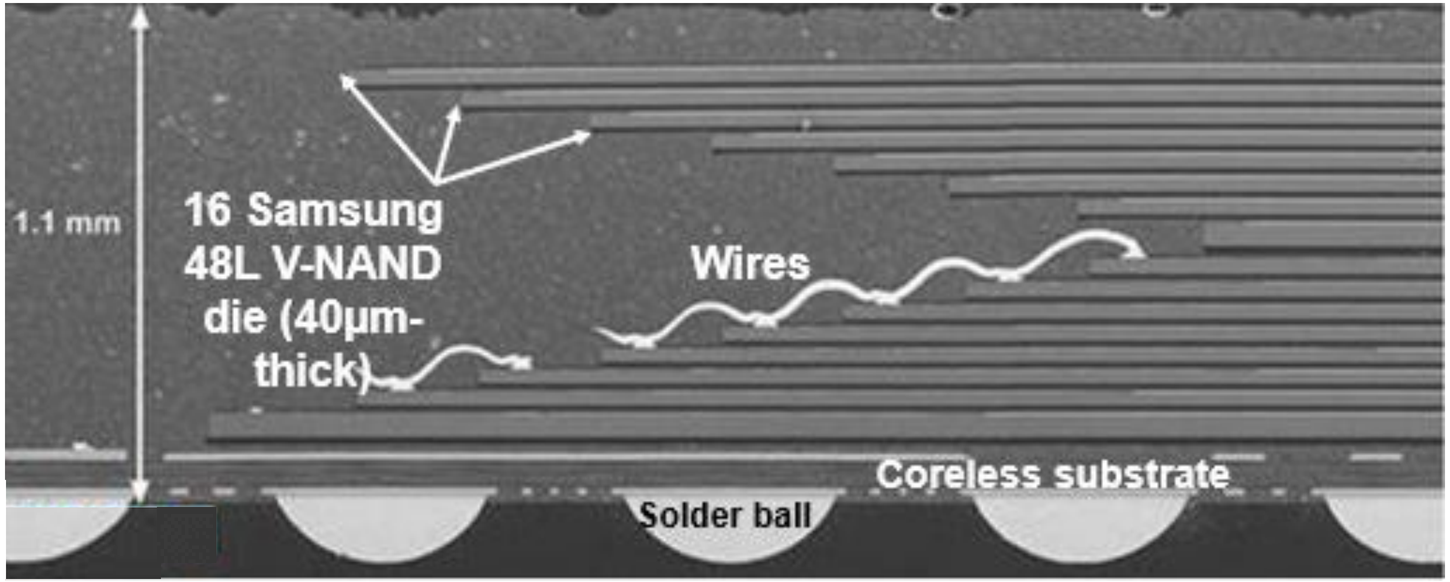
(a)





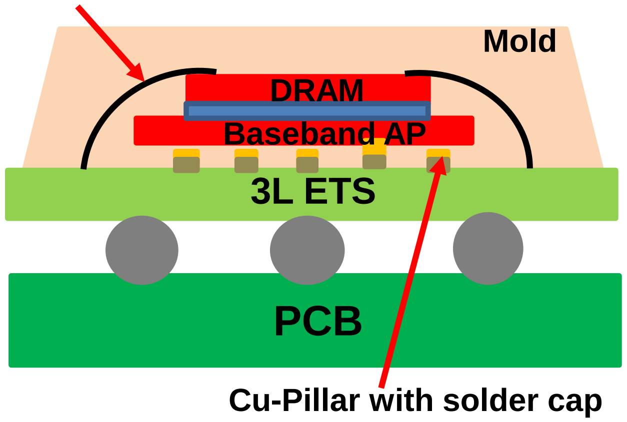
(b)

(c)



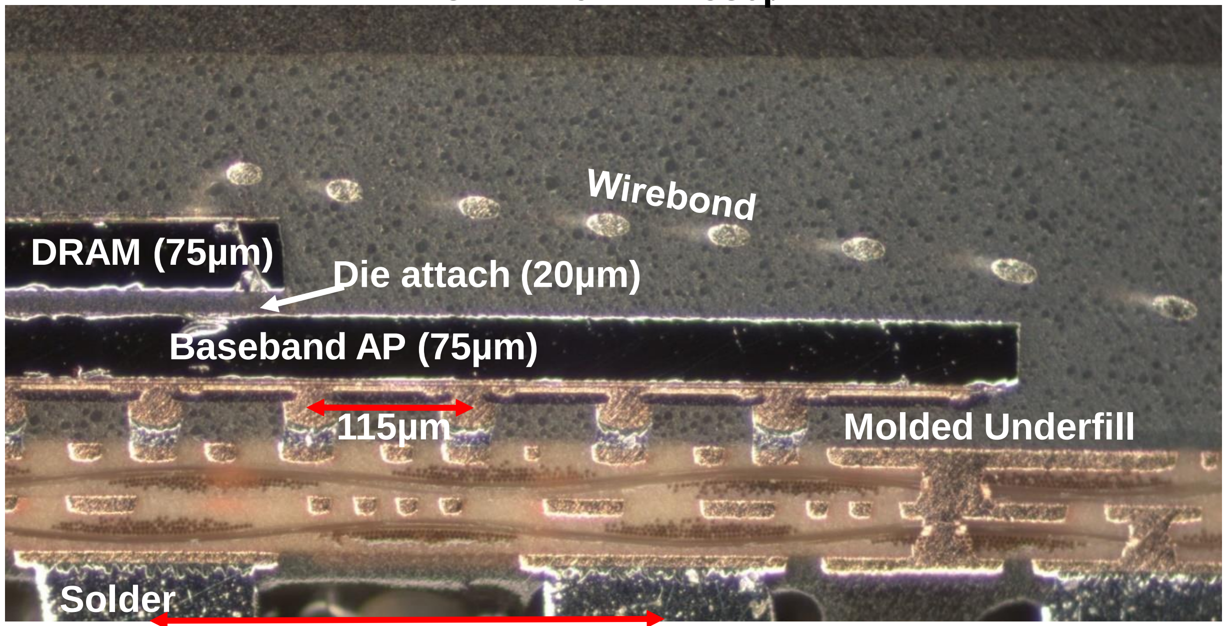
Semiconductor Advanced Packaging, 2021

3D (Flip Chip and Wirebond) Packaging

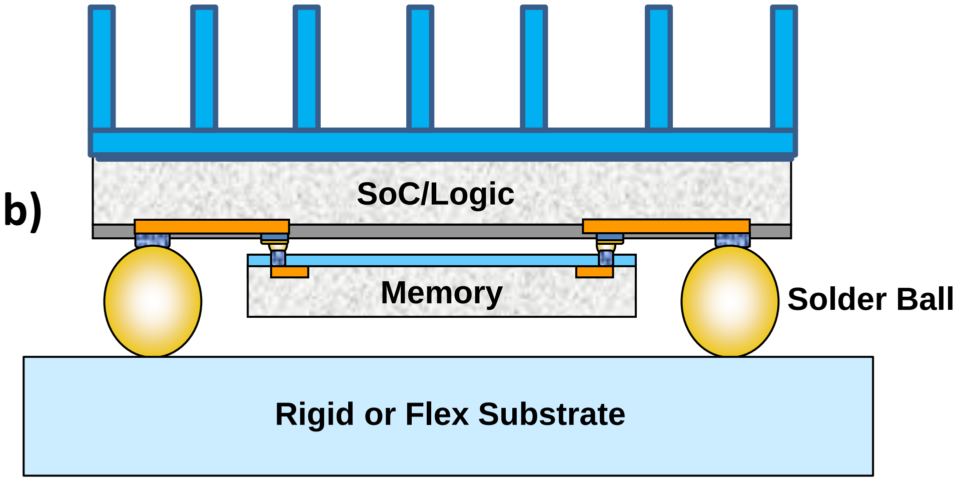


(a)

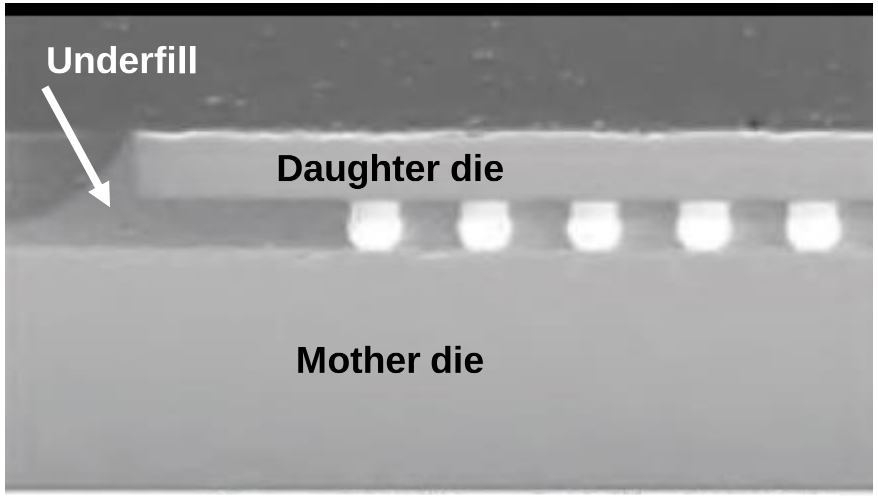
8mm x 9mm x 580µm



0.35mm

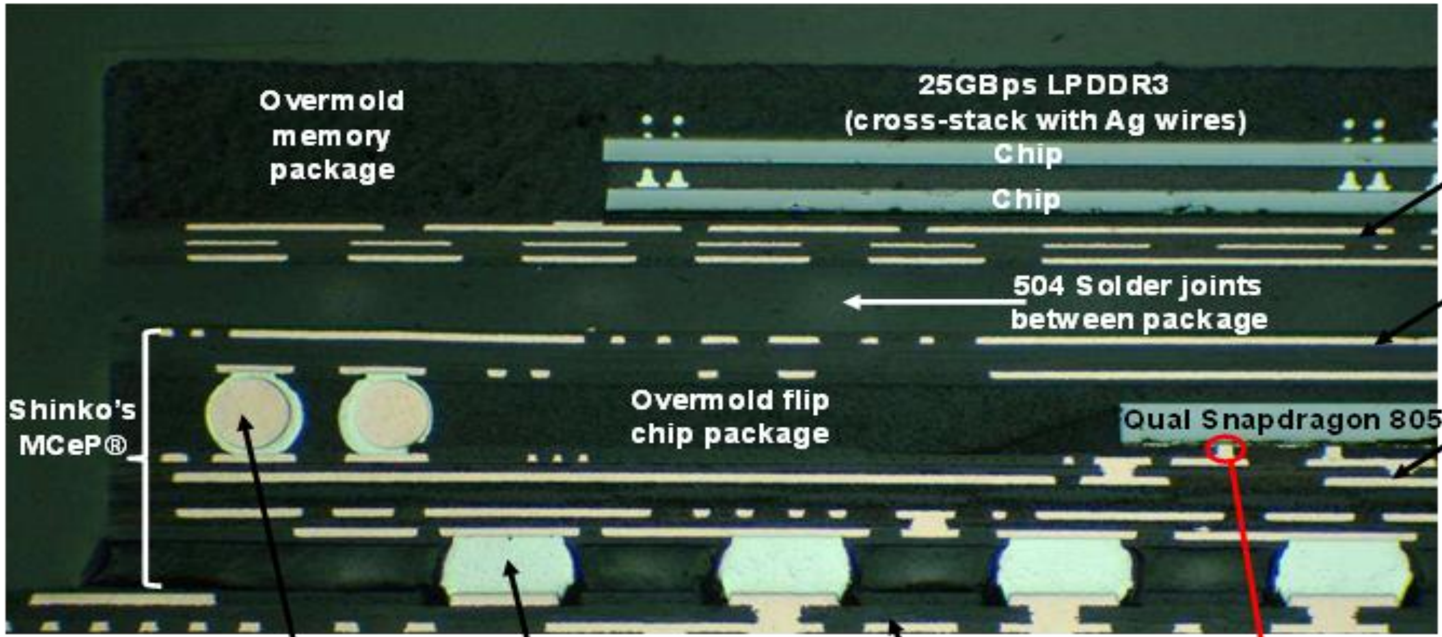


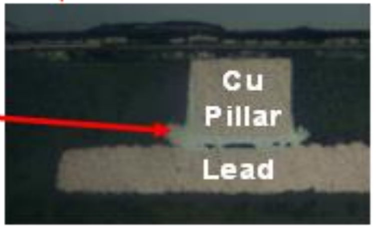
(b)



Semiconductor Advanced Packaging, 2021

3D (PoP with flip chip) IC Packaging (Qualcomm)

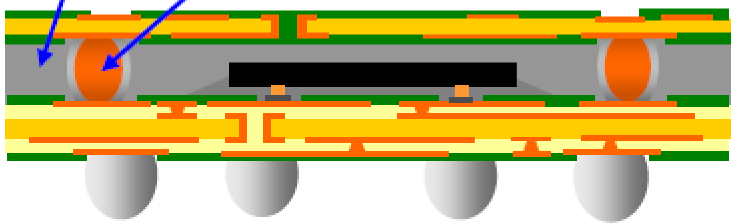




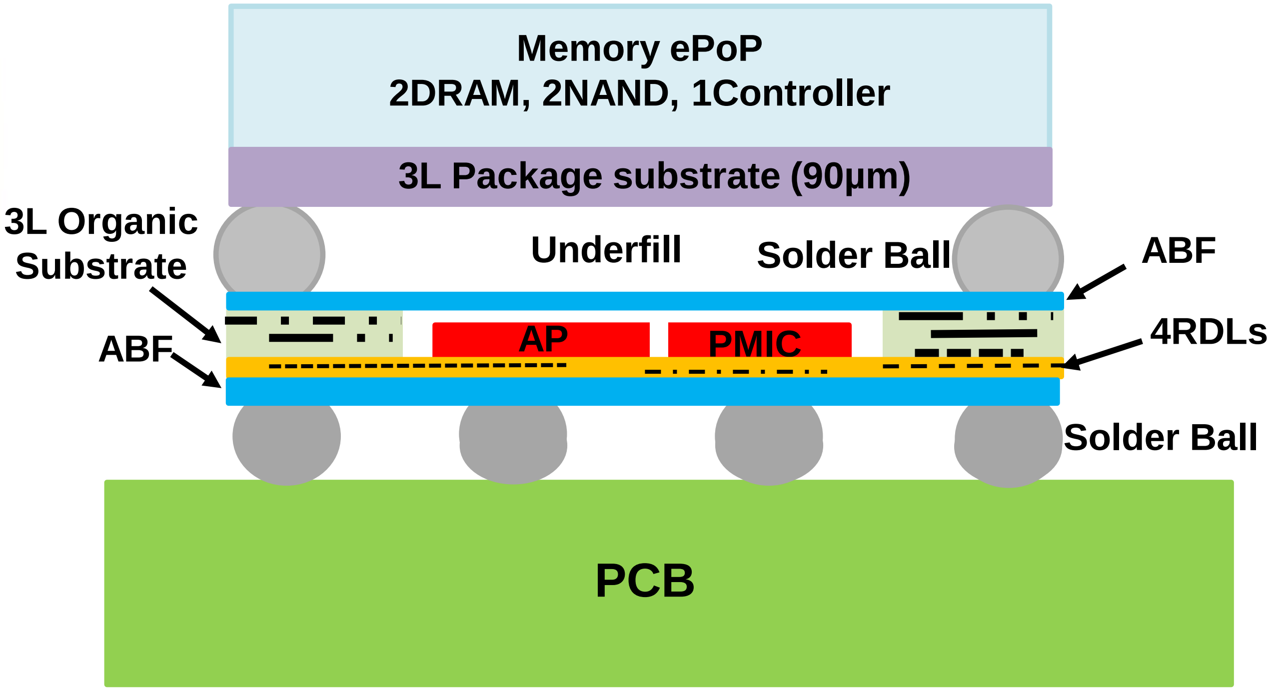
Snapdragon 805 Processor:

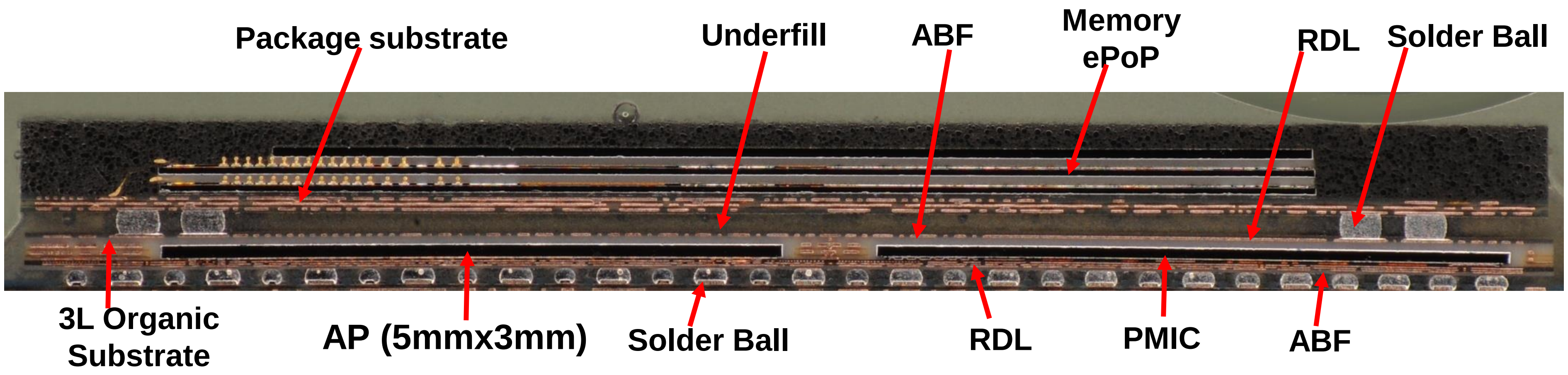
- ❑10.9mm x 11mm x 95µm
- ❑CuSnAg bumps @110µm pitch
- ❑30µm bump-height after TC-NCP

Shinko's MCeP



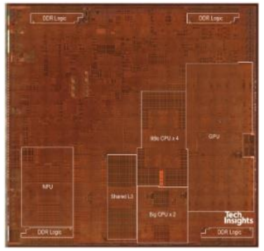
3D (PoP with Fan-Out) IC Packaging (Samsung)





3D (PoP with Fan-Out) Packaging (Apple/TSMC)

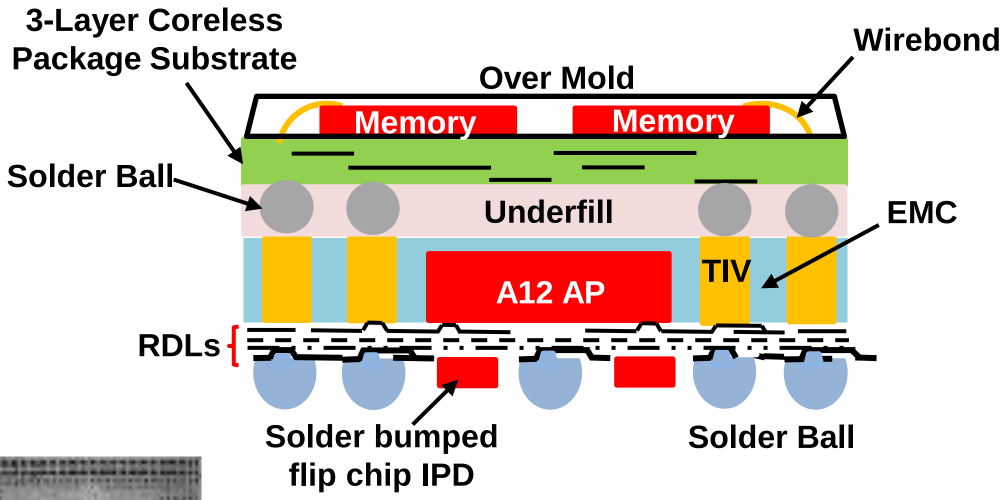
AP SoC

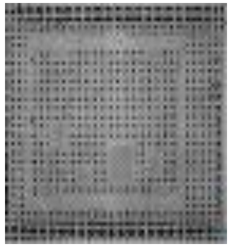


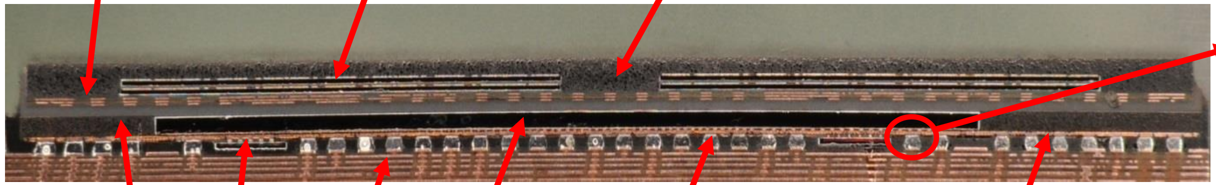
9.9mm x 8.4mm

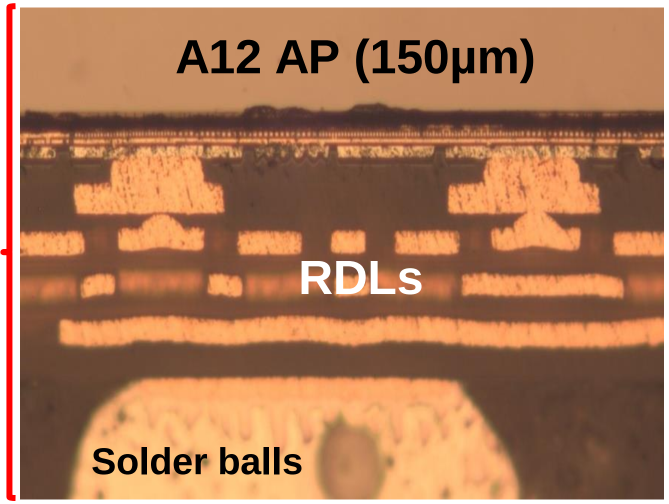
PoP

13.4mm x 14.4mm





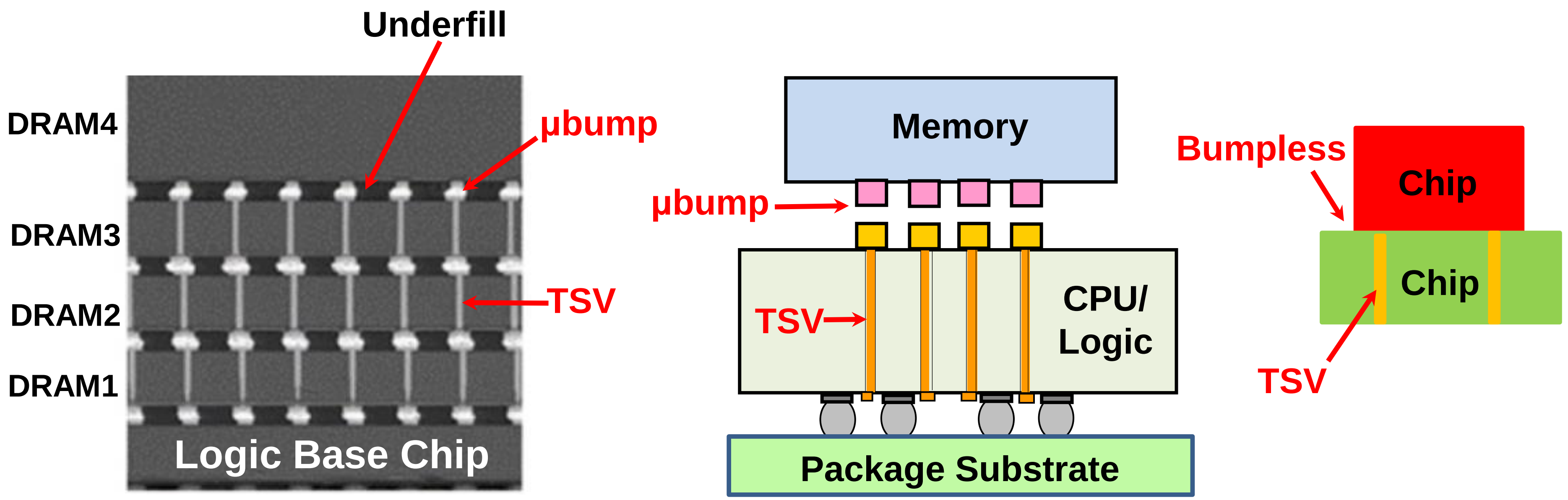




Semiconductor Advanced Packaging, 2021

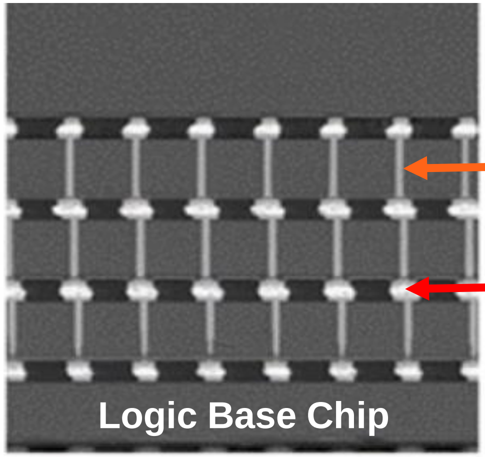
3D IC Integration (with TSVs)

3D IC Integration

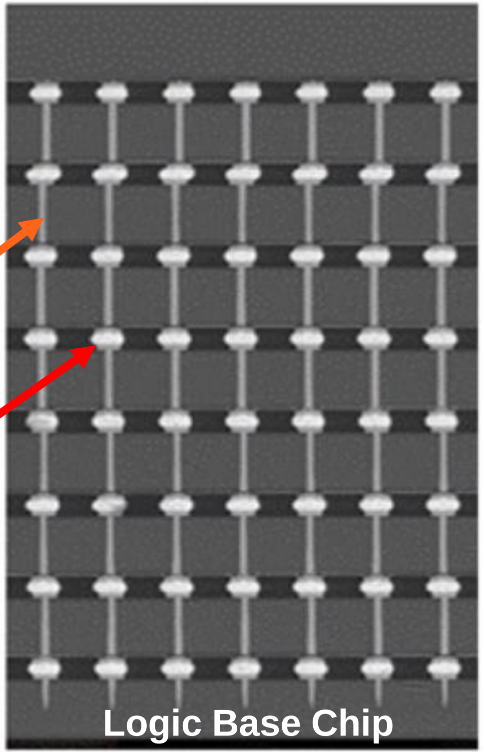


(a) (b) (c)

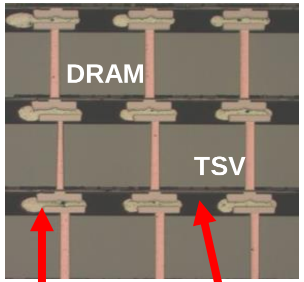
3D IC Integration with Active Interposer (High Bandwidth Memory)



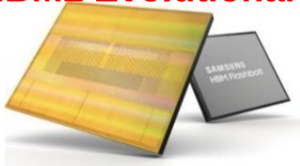
HBM (high bandwidth memory)



HBM2

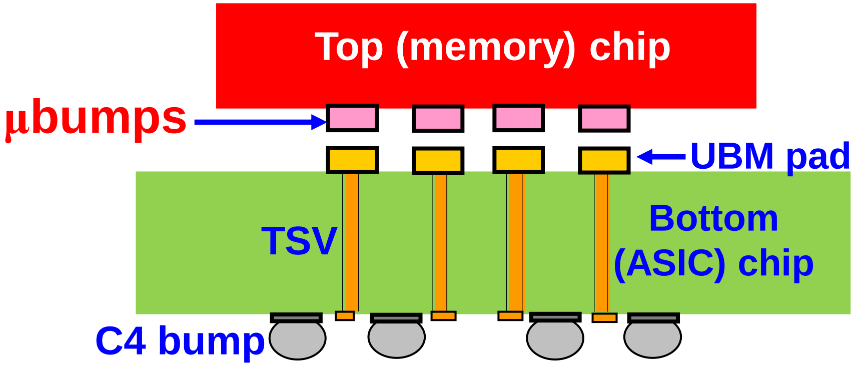


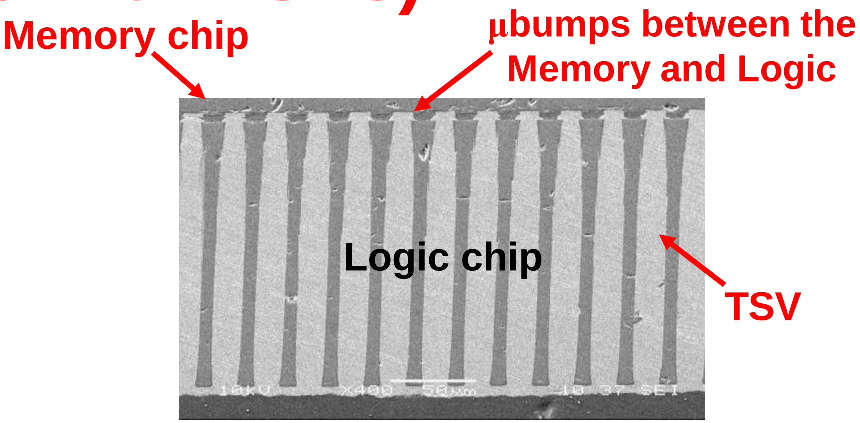
HBM2E
(HBM2 Evolutionary)

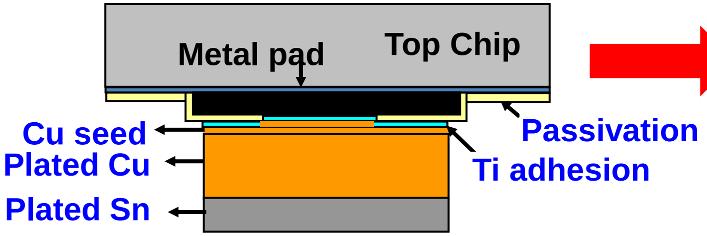


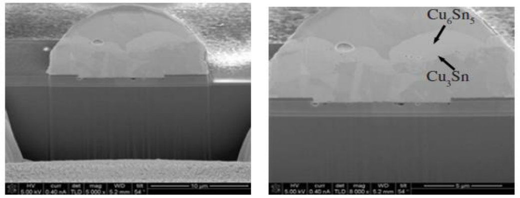
	HBM	HBM2 (Original)	HBM2/HBM2E (Current)	HBM3 (Upcoming)
Max Pin Transfer Rate	1Gbps	2Gbps	2.4Gbps	?
Max Capacity	4GB	8GB	24GB	64GB
Max Bandwidth	128GBps	256GBps	307GBps	512GBps

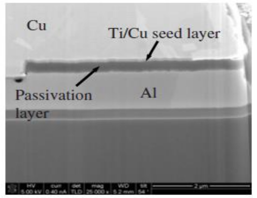
3D IC Integration with Active Interposer (Chip on Chip with TSVs)

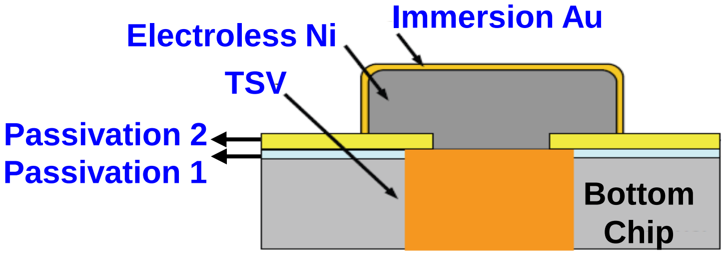


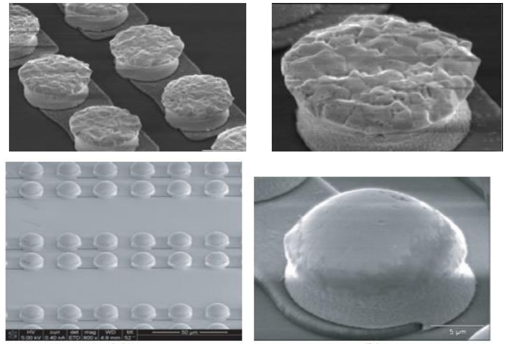












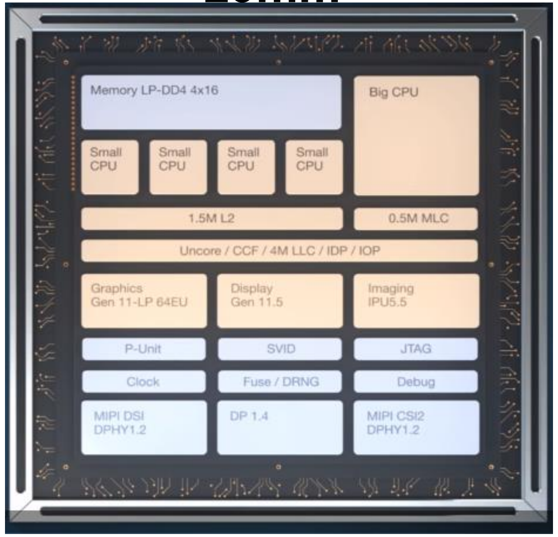
IEEE Trans. on CPMT, 2011

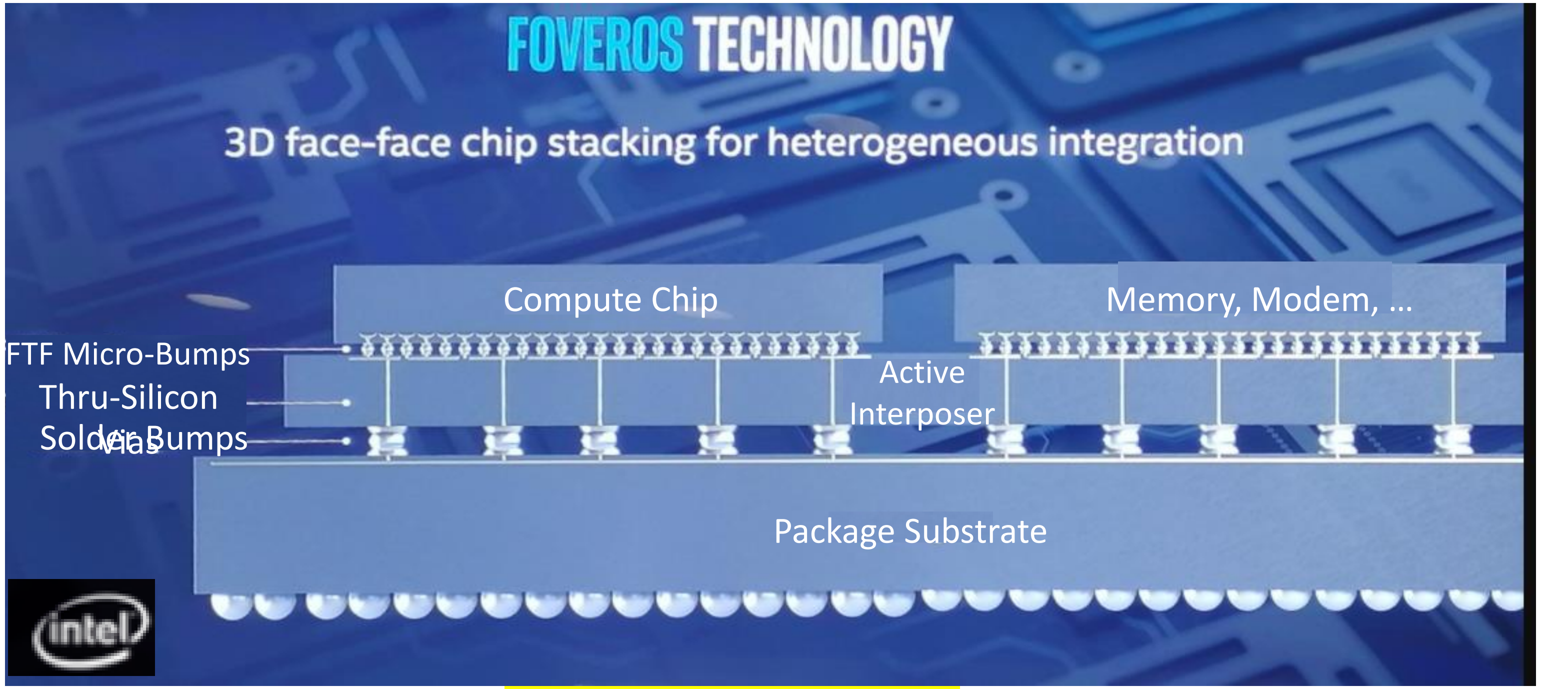
Intel 3D IC Integration – FOVEROS Technology

Lakefield

10mm

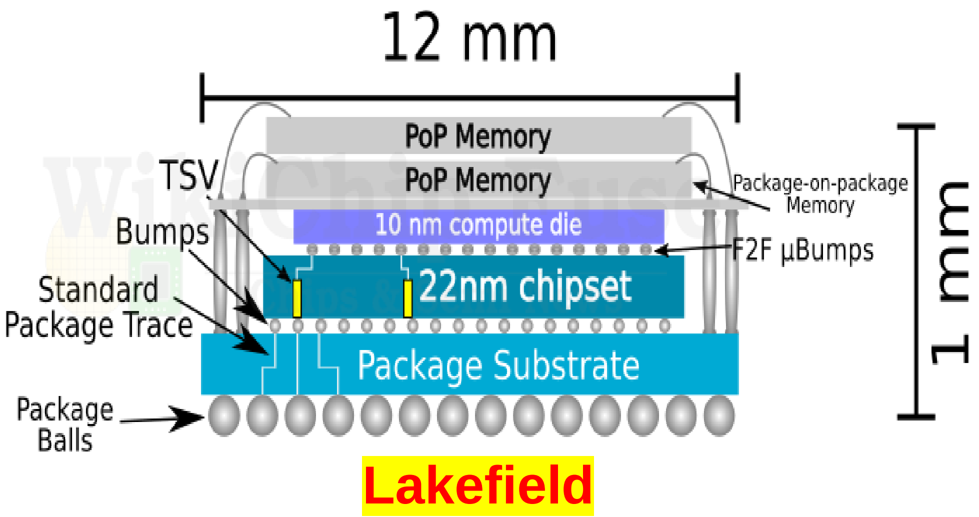
10mm

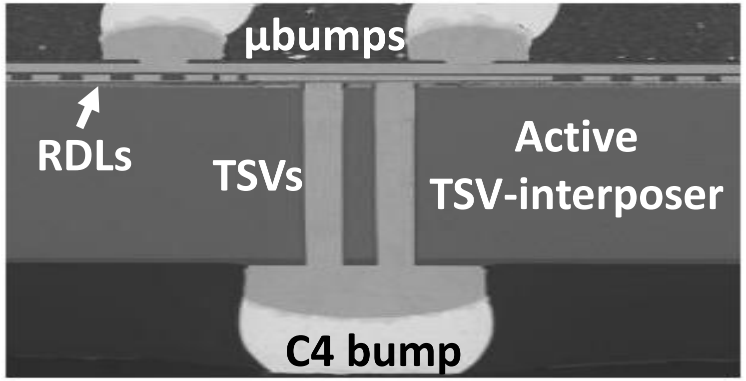


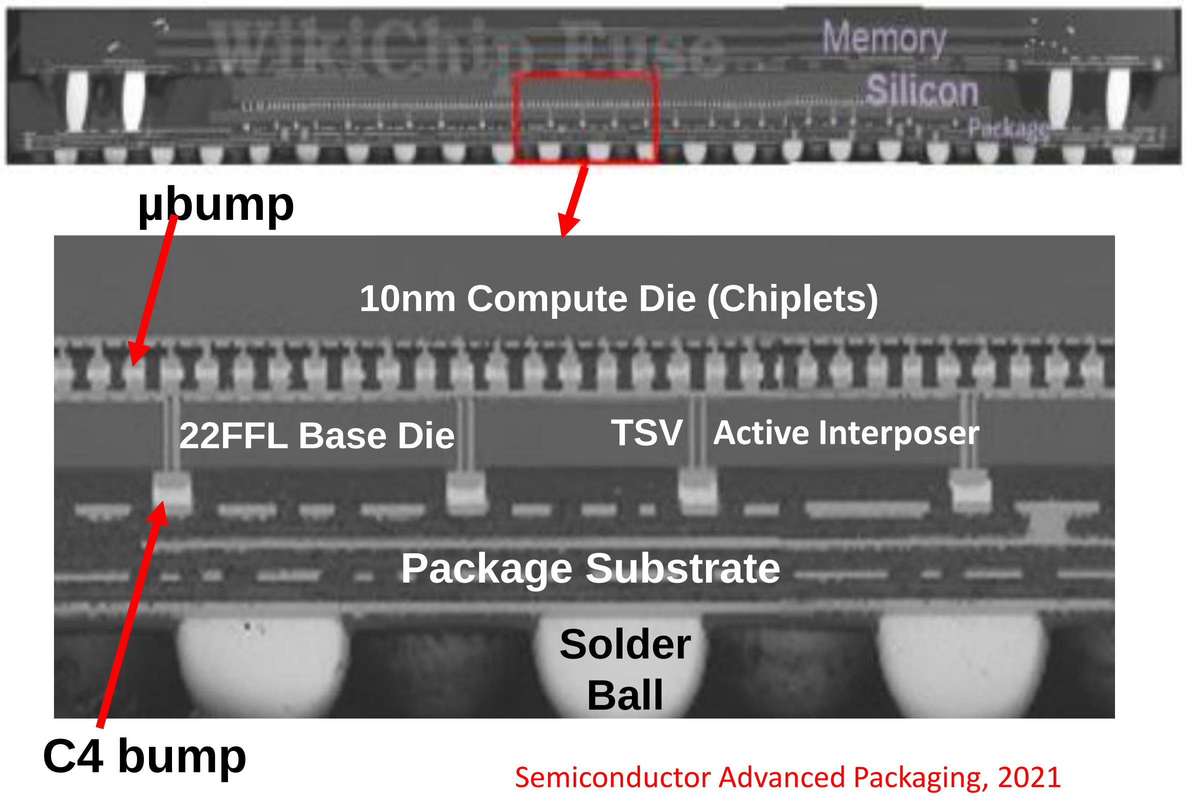


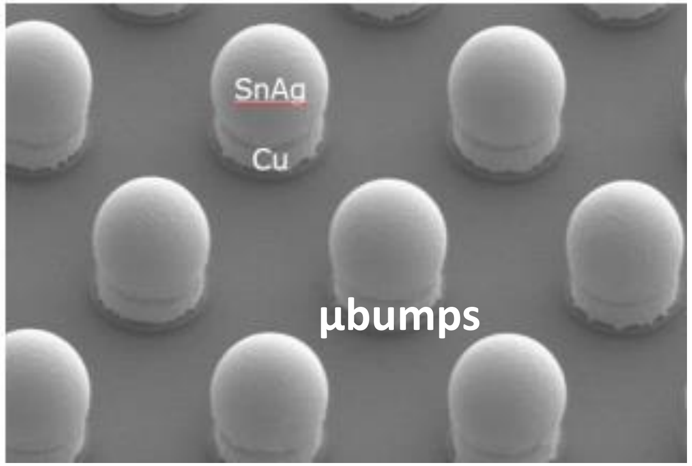
3D IC Integration

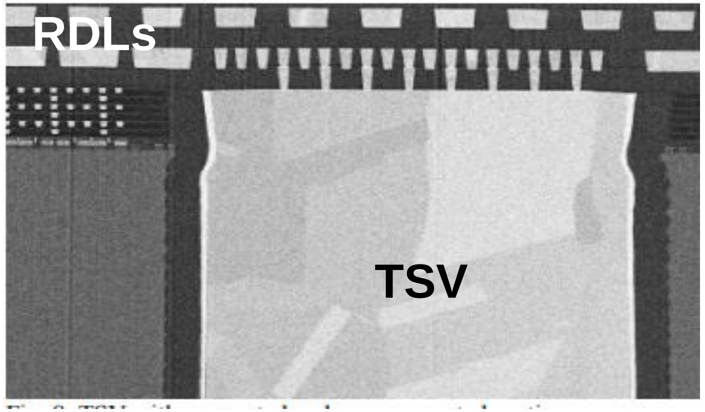
Intel 3D IC Integration – FOVEROS Technology





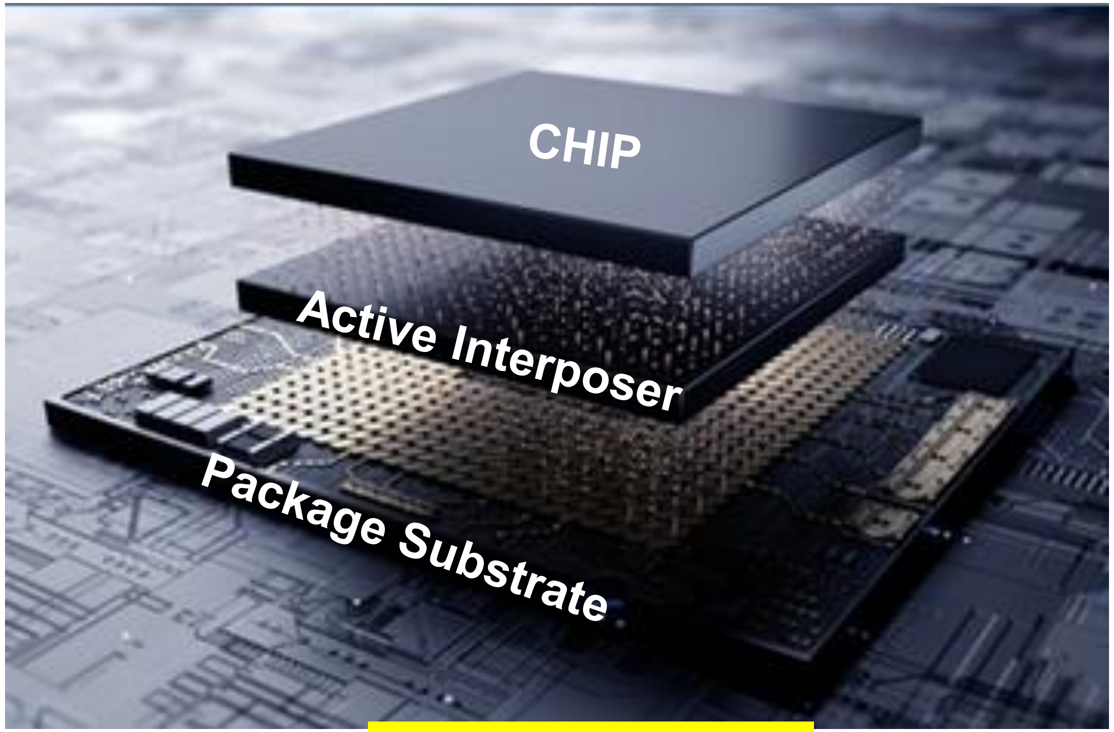






Semiconductor Advanced Packaging, 2021

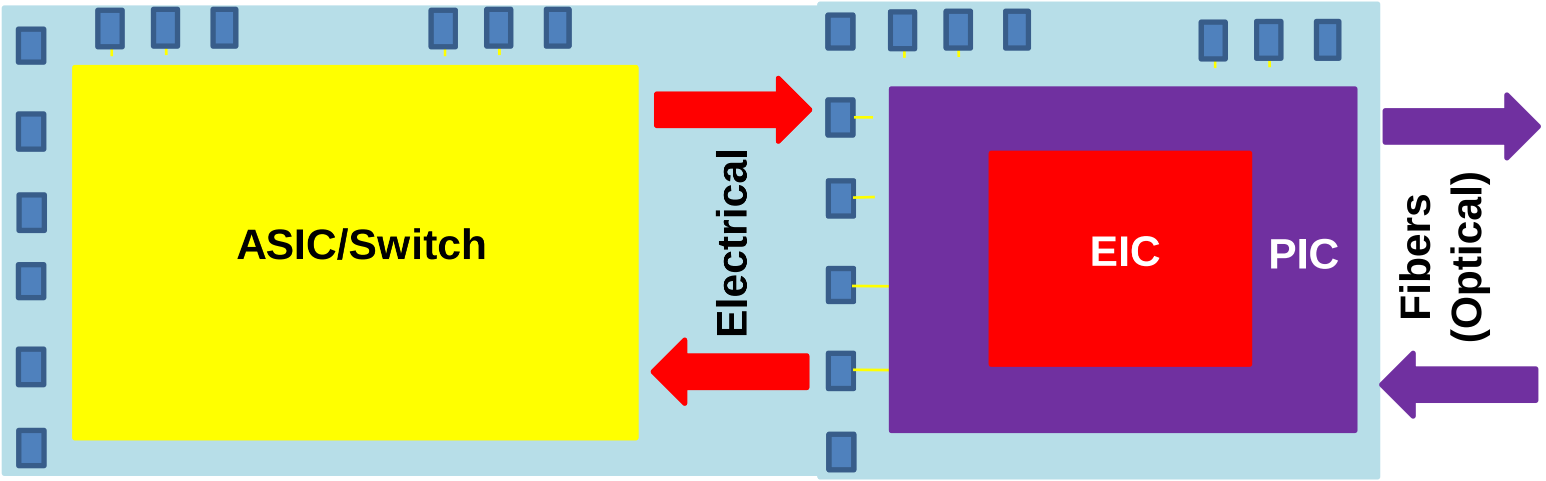
Chip-to-Active TSV-Interposer (Samsung X-Cube)

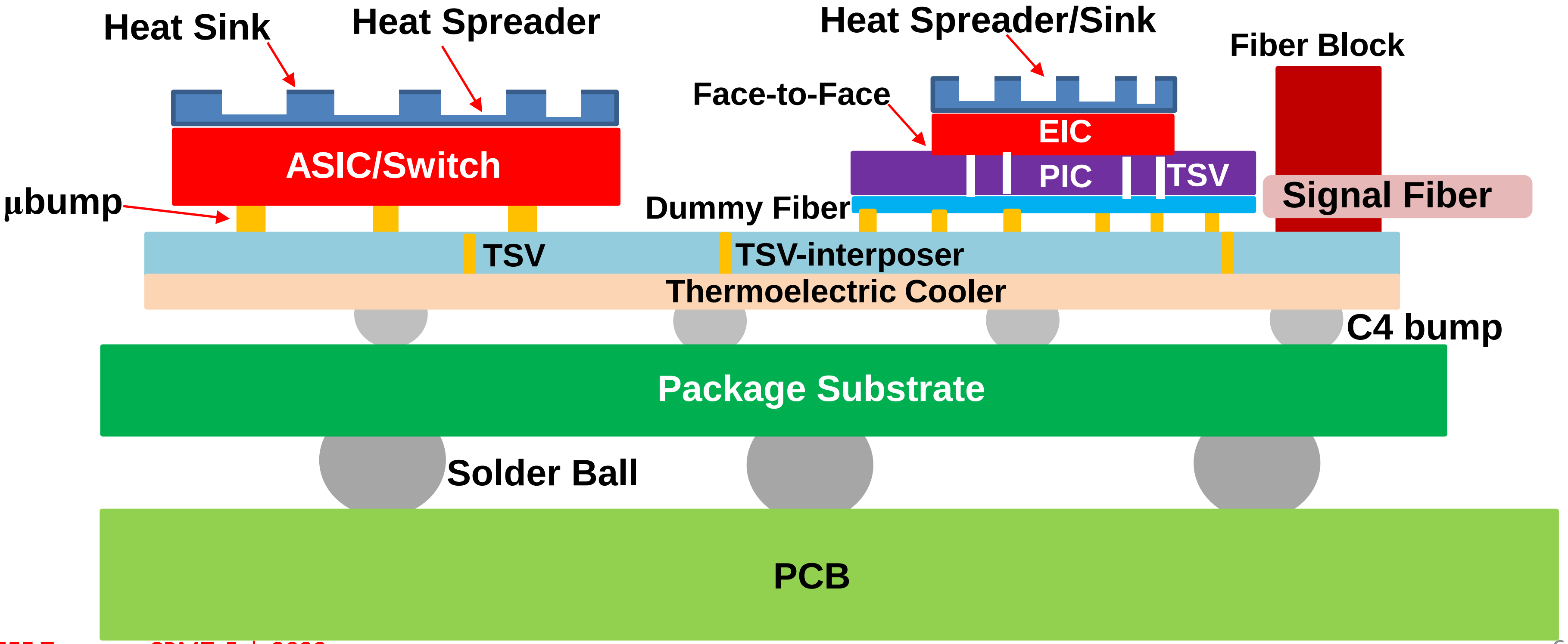


3D IC Integration

IEEE Hot Chip Conference2020.

3D Heterogeneous Integration of EIC and PIC Devices





SUMMARY

- Advanced packaging has been defined, and the kinds of advanced packaging have been ranked according to their interconnect density and electrical performance and grouped into 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration.
- The 2D IC integration, such as SiP, is and still will be used the most.
- The challenge of 2.1D IC integration (with thin film layers on build-up package substrate) is manufacturing yield.
- The 2.3D IC integration is creeping into production.
- For extreme high-performance and high-density applications, 2.5D IC integration is the solution.
- The 3D IC integration are already in volume production for mobile processors, and they will be used for more different kinds of products.
- Fan-outs, such as chip-first (face-down) and chip-first (face-up), have been in HVM for consuming products. Chip-first (face-down) is and will still be used the most. Chip-last or RDL-first is not in HVM yet but it will be soon.

SUMMARY

- **More than 75% of the flip-chip applications are with C4 bumps mass reflowed on organic package substrates and CUF (capillary underfill) (SiP).**
- **TCB (thermocompression bonding) of C2 bumps with small-force and CUF is getting traction because of the interest in using thin chips and thin organic substrates.**
- **No more than 25% of the flip-chip applications are for silicon-to-silicon, such as CoC, CoW, and WoW.**
- **Roadmaps of Df and Dk for low-loss dielectric materials of advanced packaging have been provided.**
- **The TSV-interposer integration platform for PIC and EIC of high-speed and high-bandwidth applications is getting lots of tractions. A couple of examples have been provided.**
- **A heterogeneous integration of AiP and baseband chipset with heat spreader/sink by chip-first with die face-down packaging for high performance and compact 5G millimeter wave system integration has been proposed.**

Chiplet Design
and
Heterogeneous Integration Packaging

John H Lau
Unimicron Technology Corporation
John_Lau@unimicron.com

The Biggest Difference between Chiplet and Heterogeneous Integration:

- **Chiplet is a Chip Design Method**

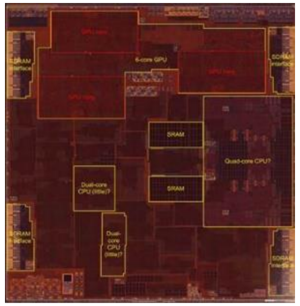
- **Heterogeneous Integration is a Chip Packaging Method**

CONTENTS

System-on-Chip (SoC)

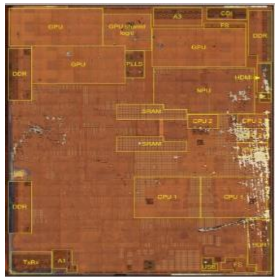
Moore's Law - Apple's Application Processors (AP):
SoC (System-on-Chip) - A10, A11, A12, A13, A14, and A15

A10



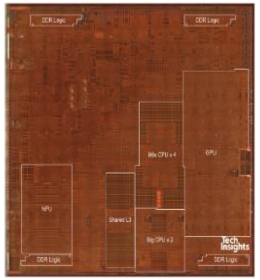
A10 consists of:
- 6-core GPU (graphics processor unit)
- 2 dual-core CPU (central processing unit)
- 2 blocks of SRAMs (static random access memory), etc.
- 16nm process technology
- Transistors = 3 billion
- Chip area = 125mm^2

A11



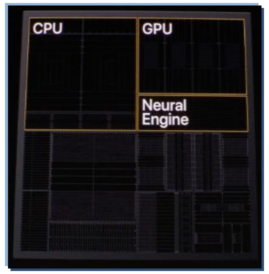
A11 consists of:
- More functions, e.g., 2-core Neural Engine for Face ID
- Apple designed tri-core GPU
- 10nm process technology
- Transistors = 4.3 billion
- Chip area =89mm^2

A12



A12 consists of:
- Eight-core Neural Engine with AI capabilities
- Four-core GPU (faster)
- Six-core CPU (better performance)
- 7nm process technology
- Transistors = 6.9 billion
- Chip area = 83mm^2

A13



A13 consists of:
- Eight-core Neural Engine with Machine Learning
- Four-core GPU (20% faster > A12)
- Six-core CPU (20% faster and 35% save energy > A12)
- 7nm process technology with EUV
- Transistors = 8.5 billion
- Chip area = 98.5mm^2

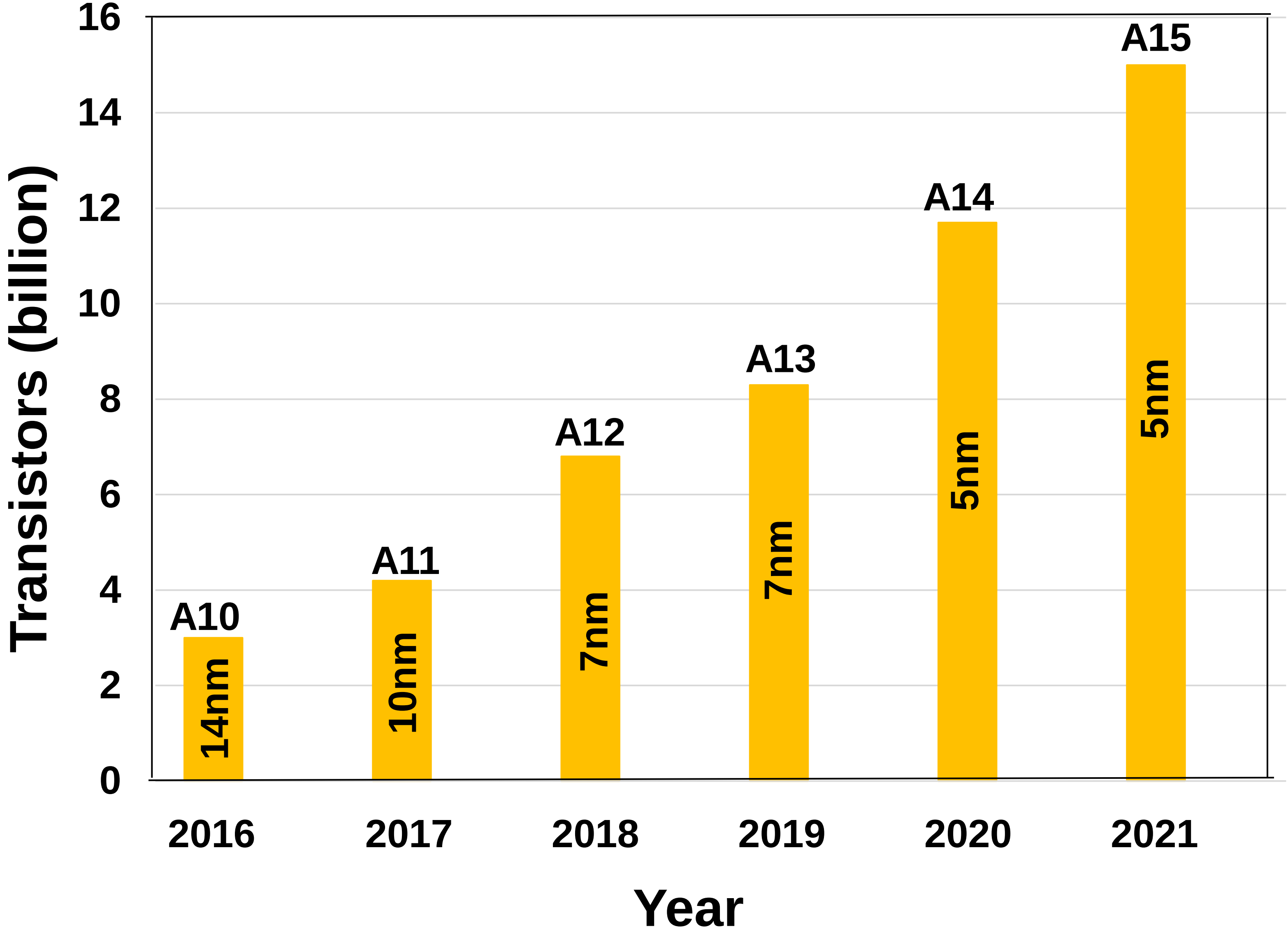
A14

A14 consists of:
- 16-core Neural Engine with Machine Learning (11 trillion/s, 10 times faster > A13)
- Four-core GPU (30% faster > A13)
- Six-core CPU (40% faster > A13)
- 5nm process technology with EUV
- Transistors = 11.8 billion
- Chip area = 88mm^2

A15

A15 consists of:
- 16-core Neural Engine to speed up AI tasks with Machine Learning (15.8 trillion/s)
- Four-core GPU, but 5-core for iPhone Pro and 13Pro Max
- Six-core CPU (faster > A14)
- 5nm process technology with EUV
- Transistors = 15 billion
- Image signal processor

Apple Application Processors vs. Transistors vs. Process Technologies (The Power of Moore's Law)

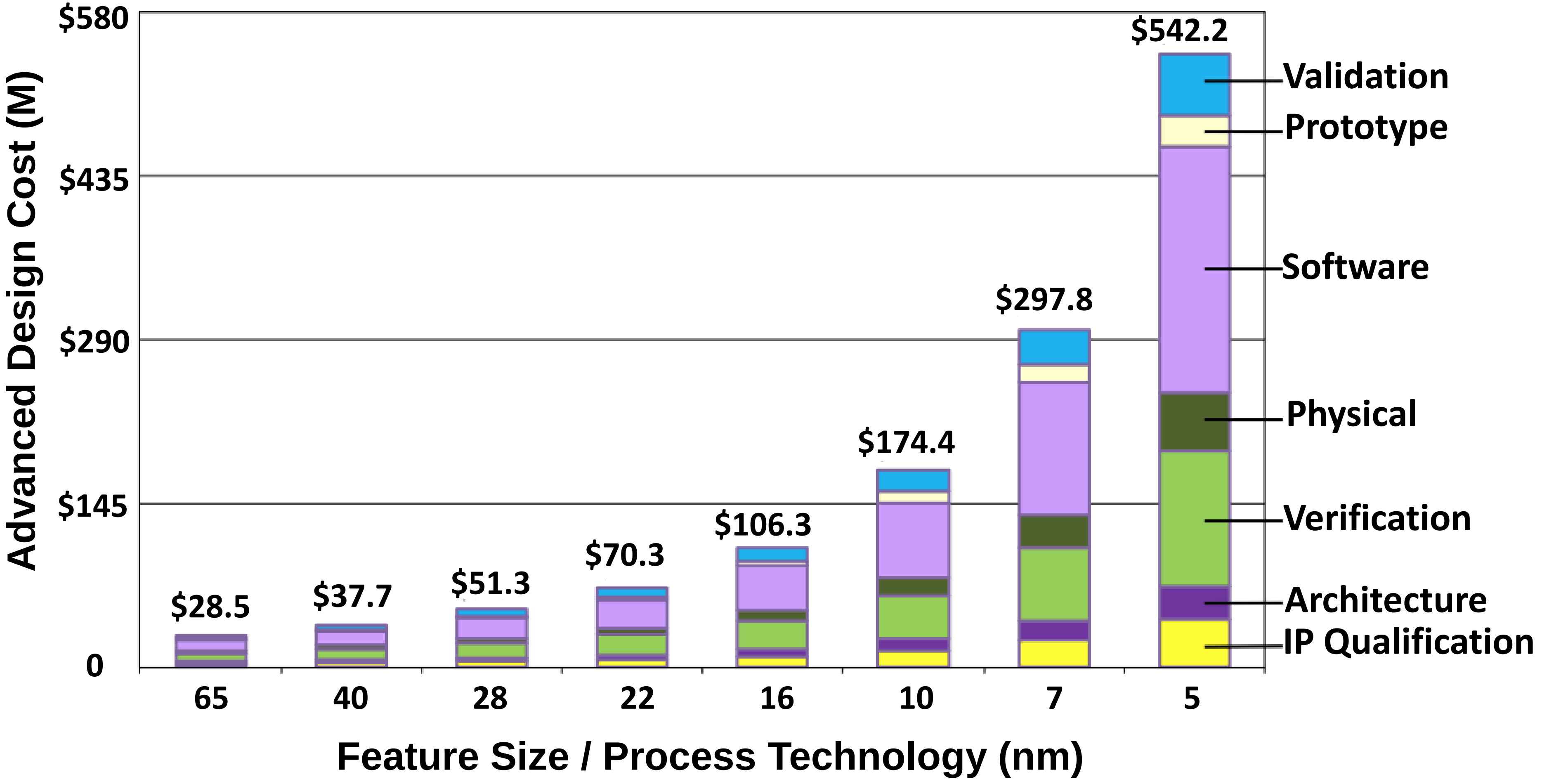


It is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC.

- **Cost in Advanced Chip Design**

- **Chip Size vs. Manufacturing Yield**

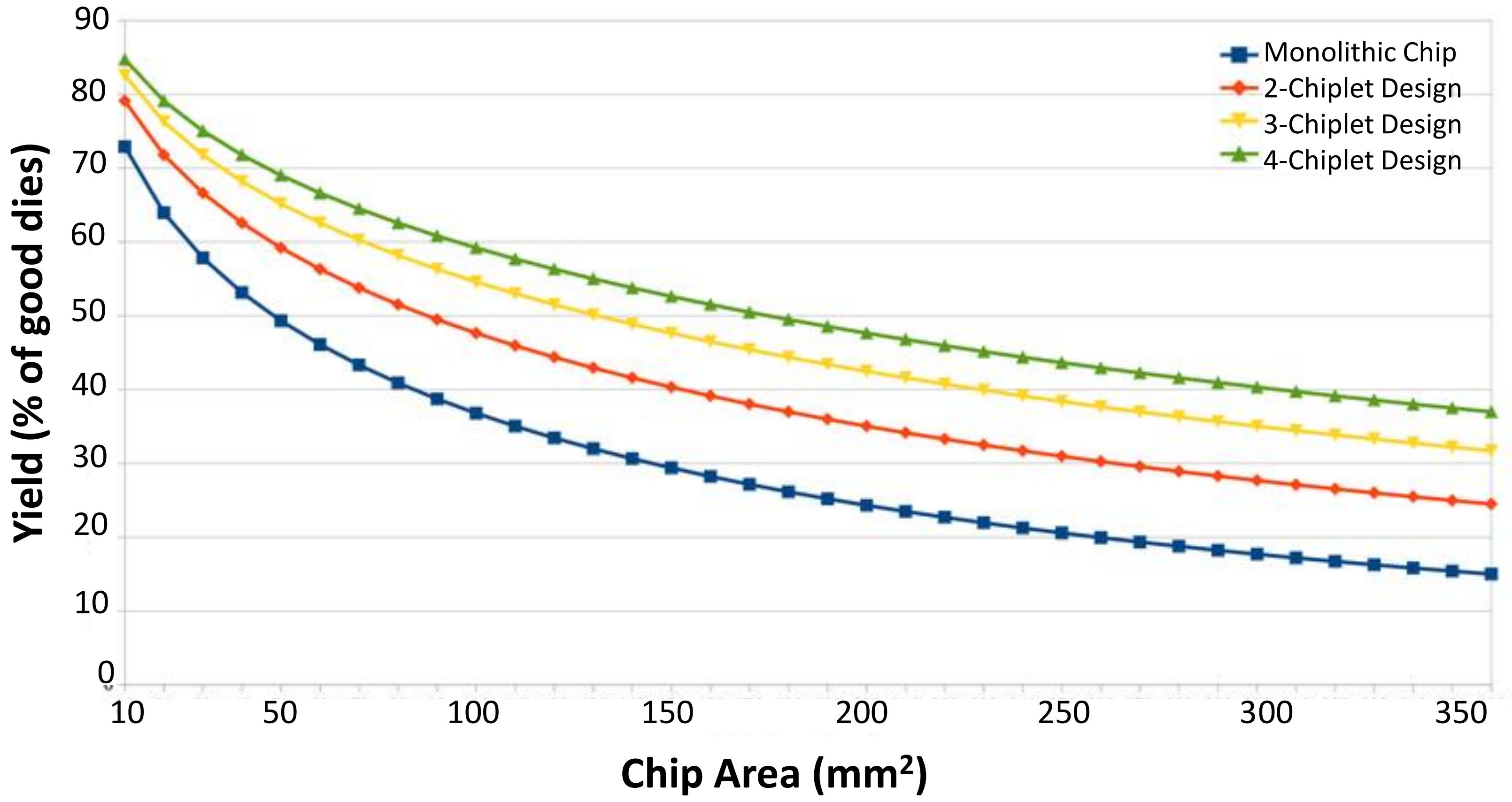
Design Cost for Advanced Nodes in Semiconductors



It will take another $1 billion for 5nm process development.

Sources: International Business Strategies

Yield (Cost) per Wafer vs. Chip Size for SoC and Chiplets



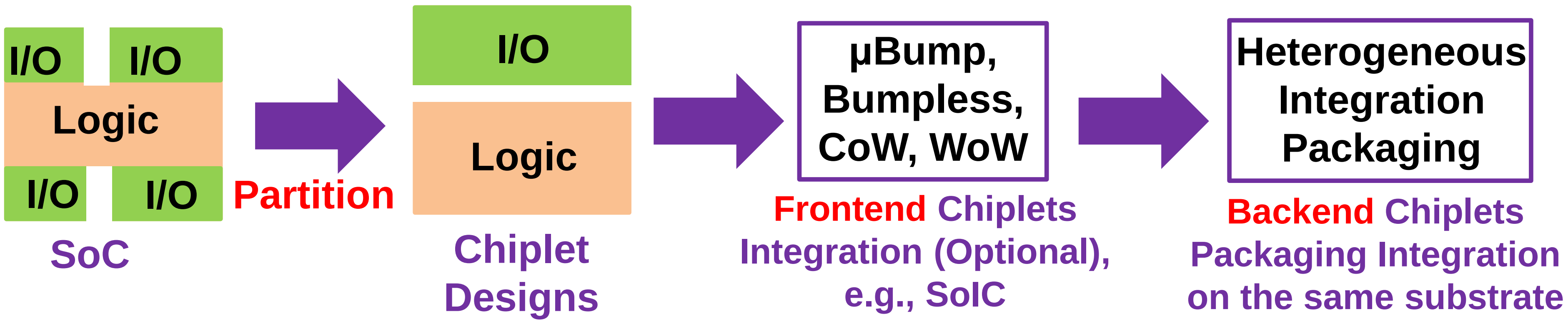
Sources: https://en.wikichip.org/wiki/chiplet, March 27, 2020.

Chiplet Design and Heterogeneous Integration Packaging

- Chip partition and integration
- Chip split and integration
- Multiple System and Integration

Chiplet Design and Heterogeneous Integration Packaging

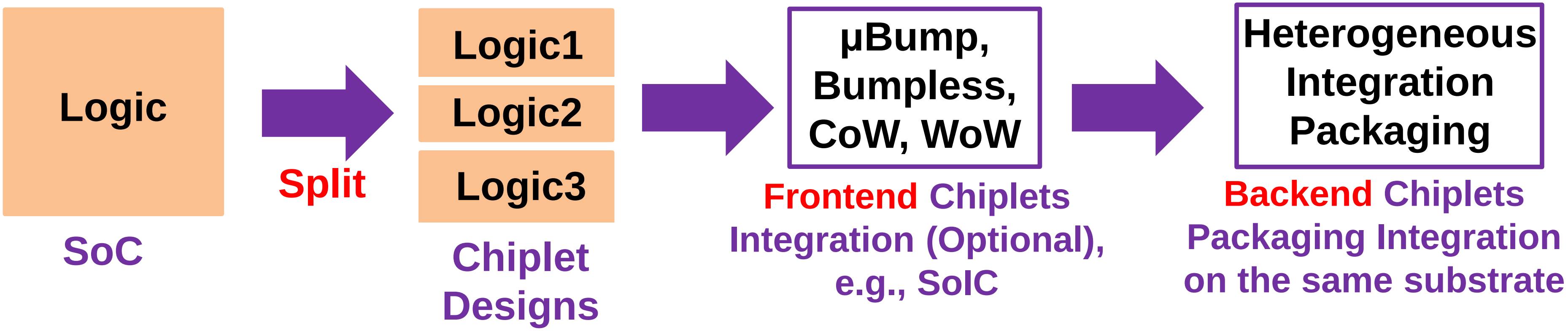
Chip partition and integration (Driven by cost and technology optimization)



Semiconductor Advanced Packaging, Springer, 2021

Chiplet Design and Heterogeneous Integration Packaging

Chip split and integration (Driven by cost and yield)



Semiconductor Advanced Packaging, Springer, 2021

Chiplet Design and Heterogeneous Integration Packaging Comparing with SoC: Advantages and Disadvantages

- The key advantages of chiplets heterogeneous integration are:
  - (1) yield improvement (lower cost) during manufacturing;
  - (2) faster time-to-market;
  - (3) cost reduction during design;
  - (4) better thermal performance;
  - (5) reusable of IP;
  - (6) modularization.

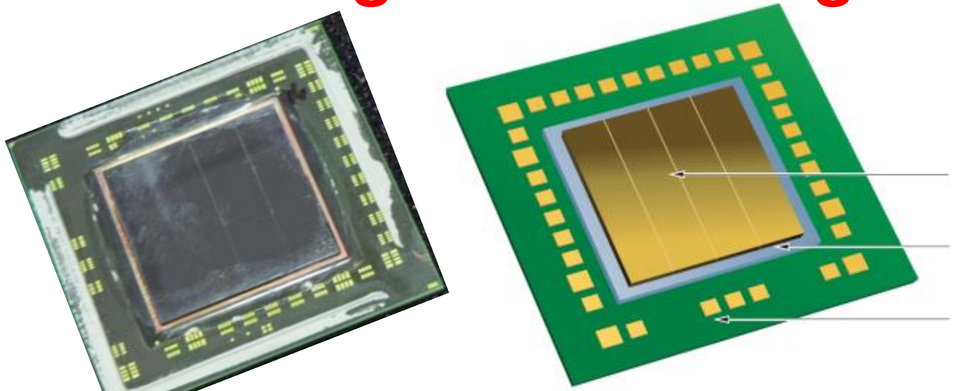
- The key disadvantages are:
  - (1) additional area for interfaces;
  - (2) higher packaging costs;
  - (3) more complexity and design effort;
  - (4) past methodologies are less suitable for chiplets.

Semiconductor Advanced Packaging, Springer, 2021

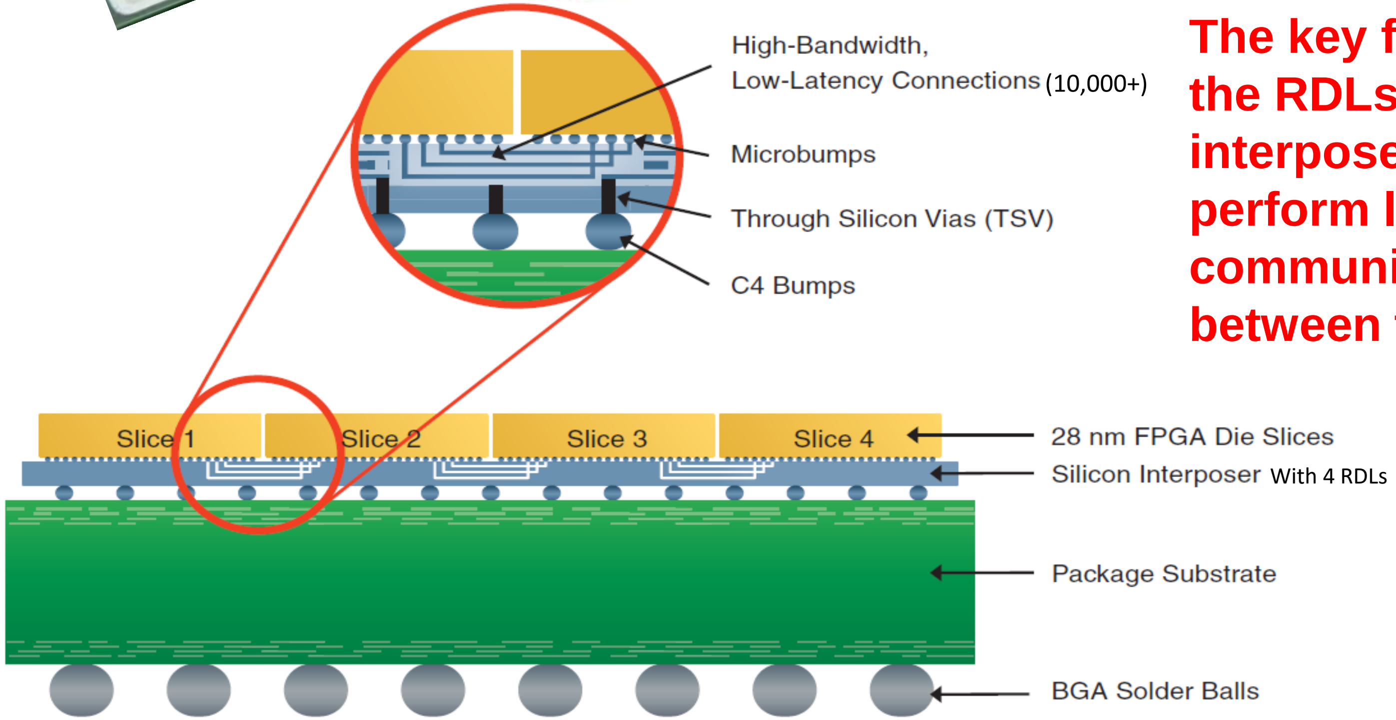
Examples on Chiplet Design and Heterogeneous Integration Packaging

- **Xilinx**
- **AMD**
- **Intel**
- **TSMC**
- **Nvidia**
- **Samsung**

Xilinx's Chiplet Design and Heterogeneous Integration Packaging



For better manufacturing yield (to save cost), a very large SoC has been split into 4 smaller chips.



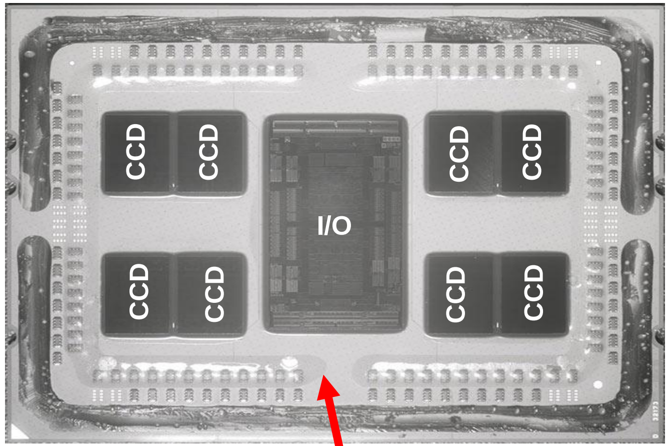
The key function of the RDLs on the interposer is to perform lateral communications between the chips.

Shipped in 2013

AMD's Chiplet Design and Heterogeneous Integration Packaging

Extreme-performance yield computing (EPYC)

2D IC Integration



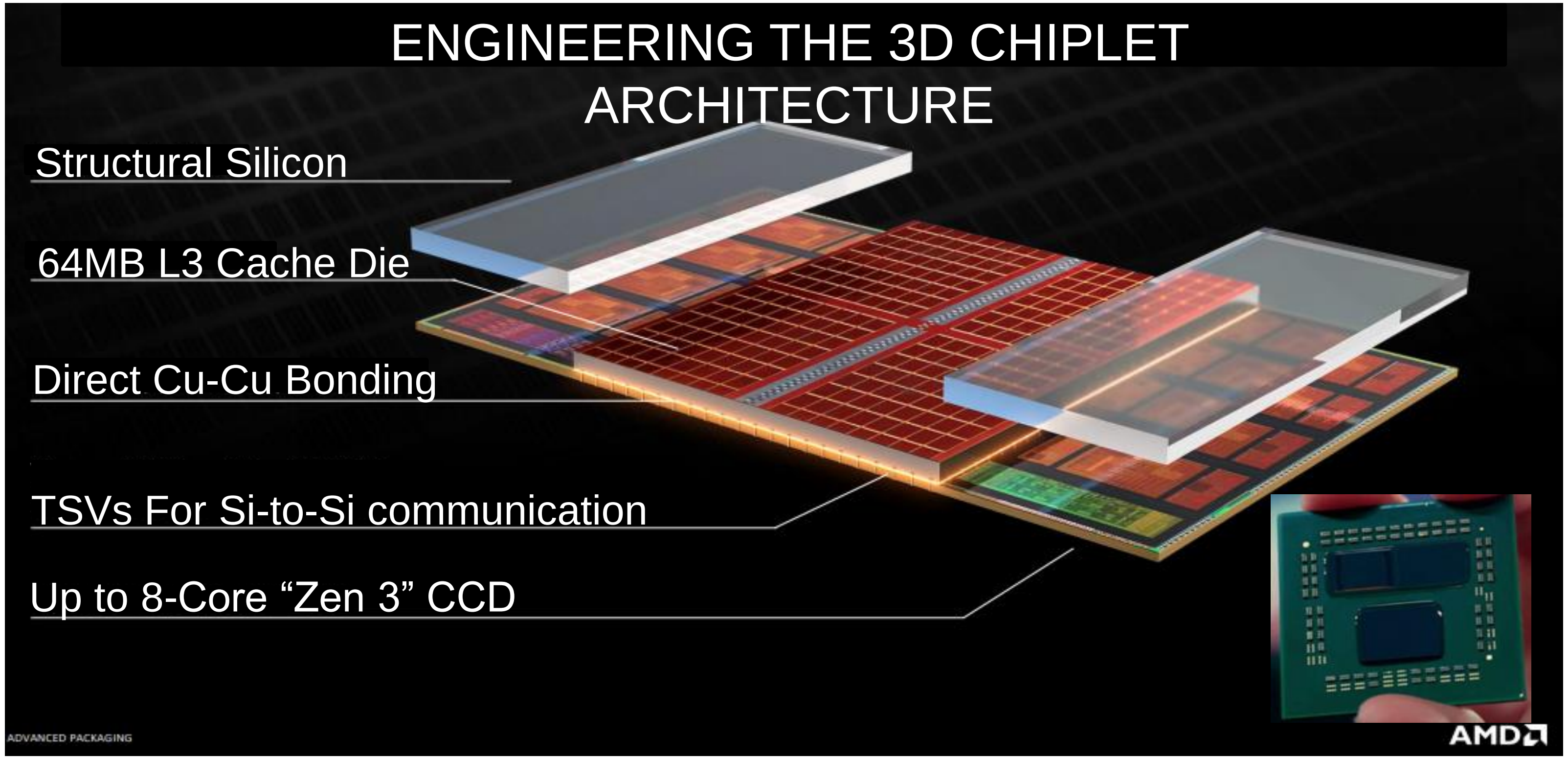
9-2-9 package substrate

- The I/O and CCD (core complex die or CPU compute die) are partitioned
- The CCD is split into two chiplets (7nm process technology)
- The I/O chip is with 14nm process technology

Shipped in 2019

AMD's Future Chiplet Design and Heterogeneous Integration Packaging

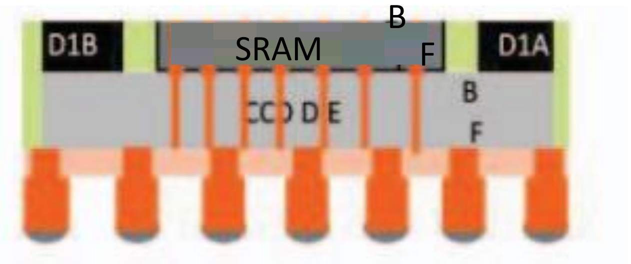
3D IC Integration

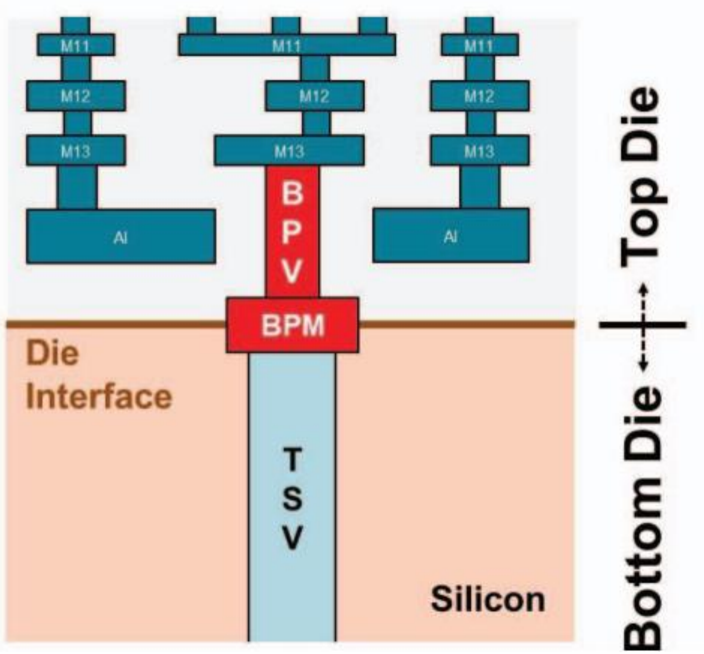


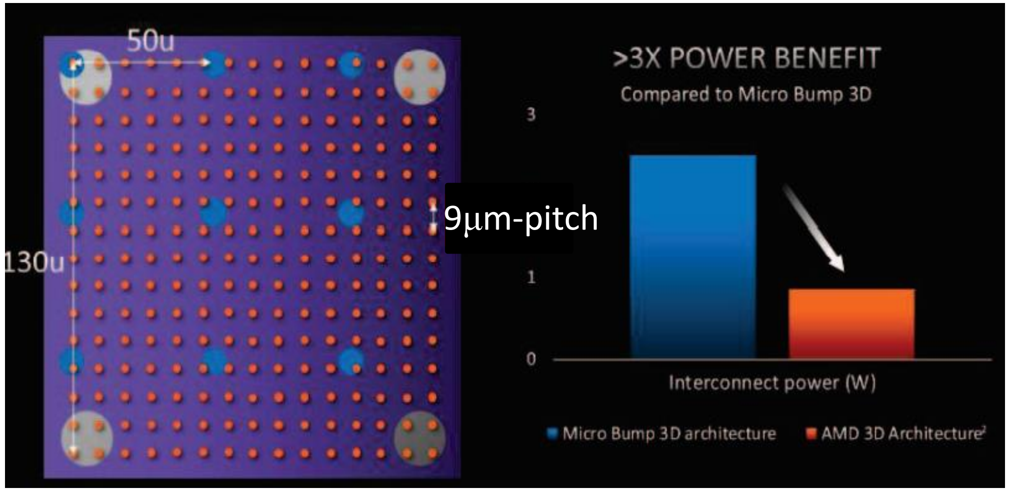
- **AMD's RYZEN 9 5900X Prototype chip for gaming**
- **Same 7nm process technology as RYZEN, but using 3D chiplet copper-to-copper bumpless hybrid bonding**

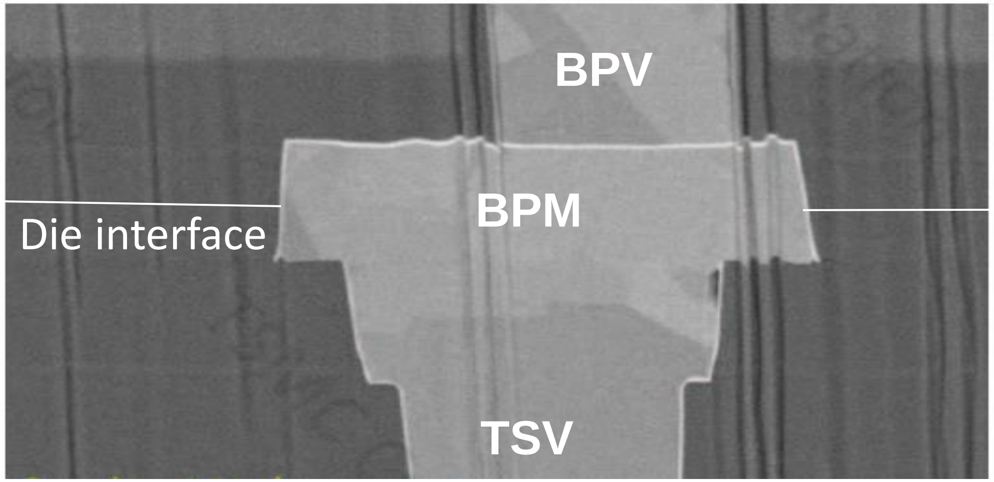
IEEE Hot Chip Conference, August 2021

AMD 3D V-Cache Hybrid Bonding: SRAM (Face)-to-CCD (Back)









TSMC's SoICs technology

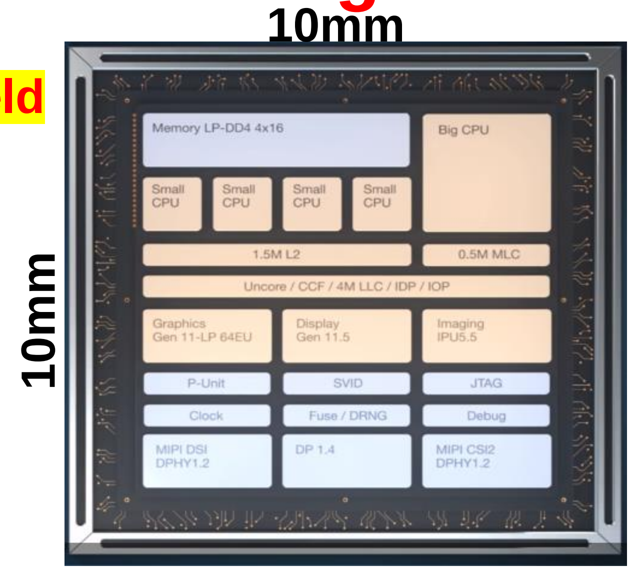
BPM (bond pad metal)
BPV (bond pad via)
TSV (through-silicon via)

ISSCC 2022 and ECTC2022

Intel’s Chiplet Design and Heterogeneous Integration Packaging

Lakefield

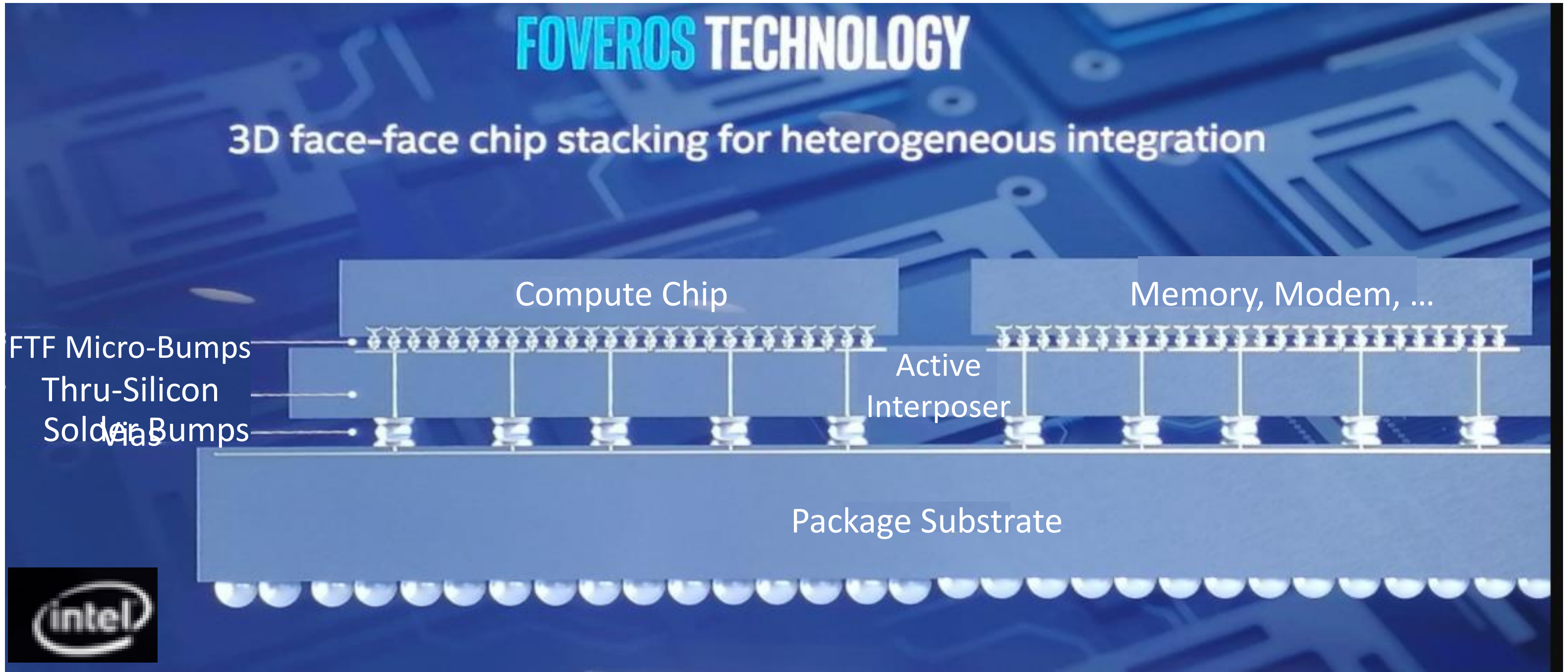
(a)



3D IC Integration

- The memory and graphics are partitioned
- The large CPU is split into 5 smaller CPUs (10nm process technology)
- All the tiles (or chiplets) are attached on an active interposer

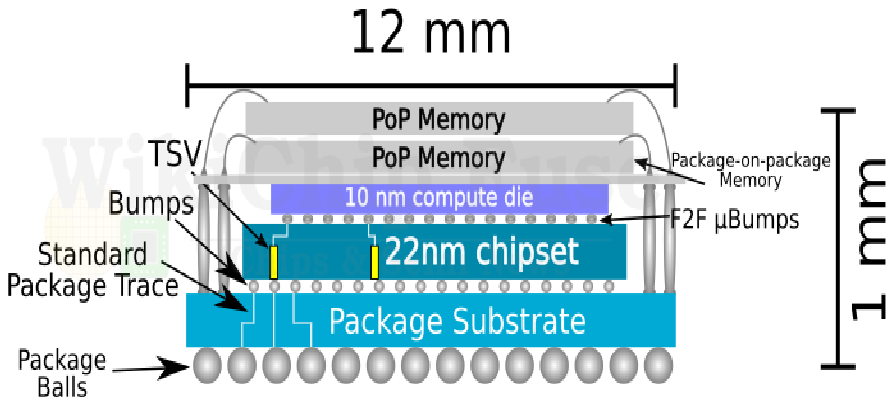
(b)



Shipped in 2020

Intel's chiplets are Face-to-Face Microbumped on the Active TSV-interposer

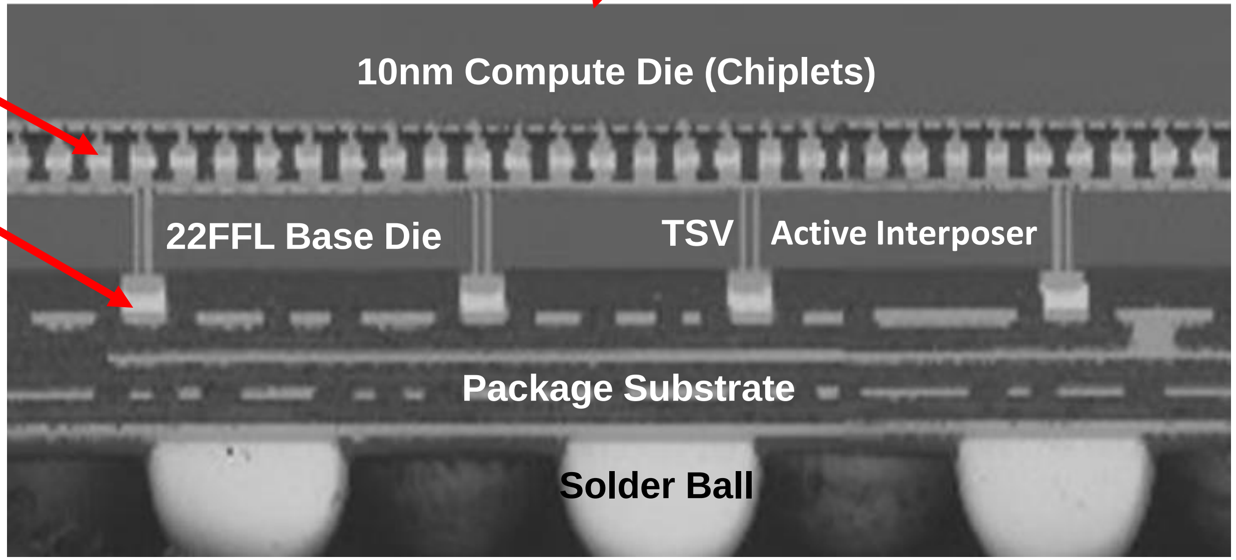
Lakefield



μbump

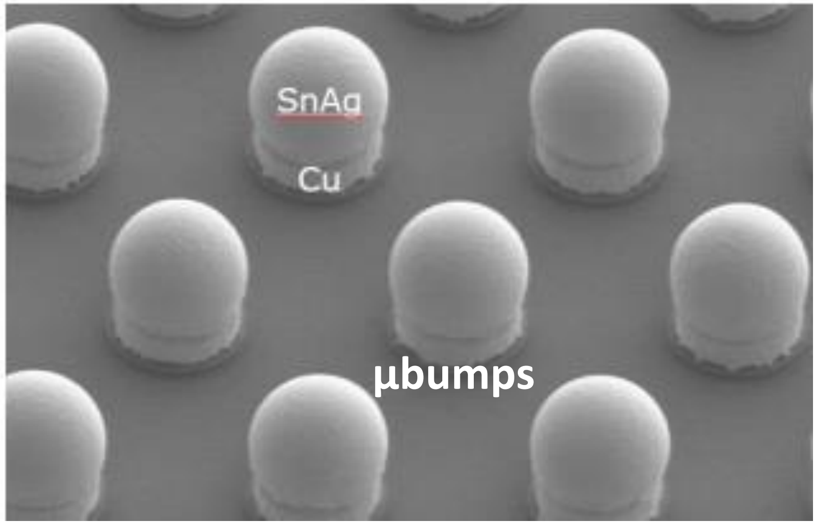
C4 bump

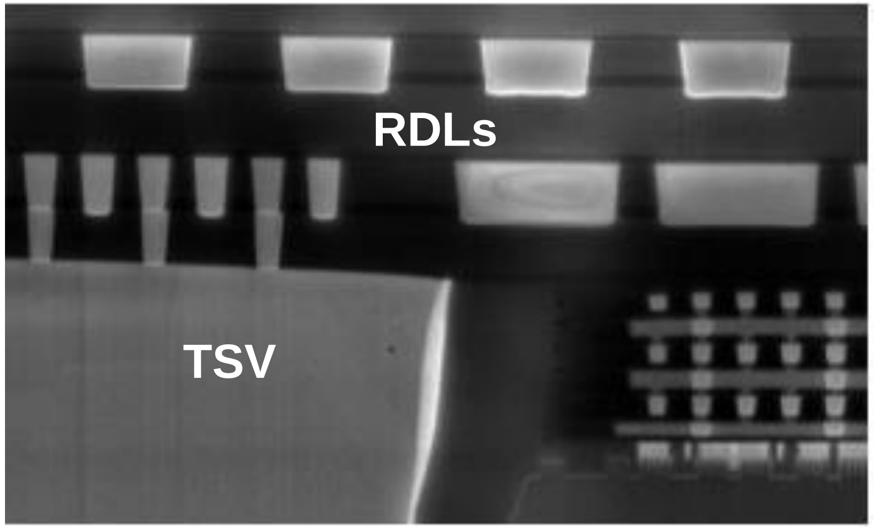
3D IC Integration

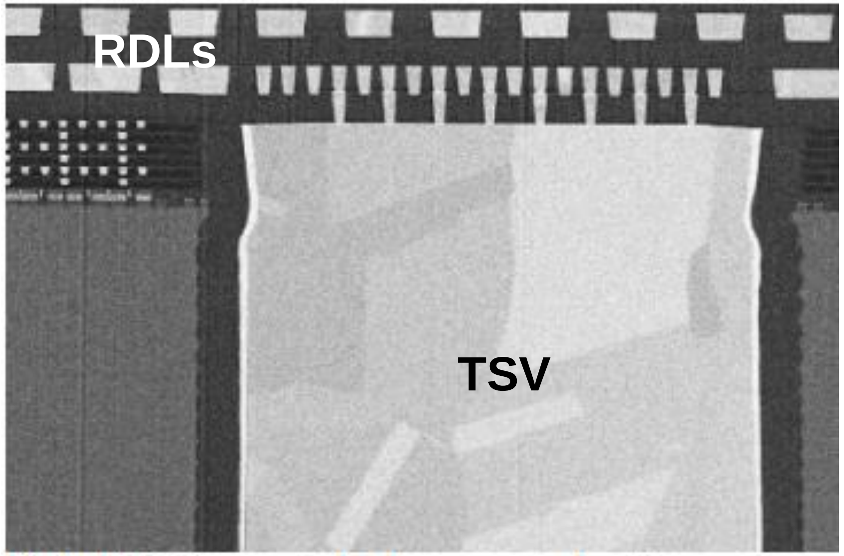


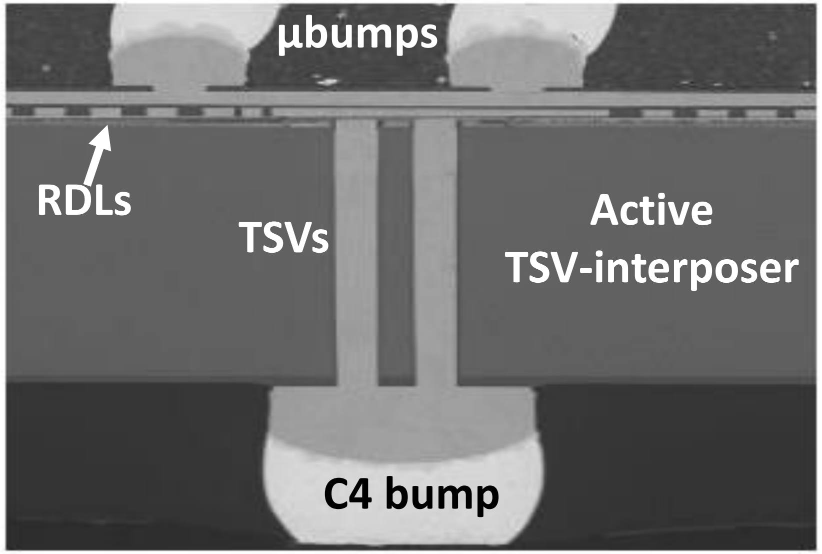
IEDM 2019 and ISSCC 2020

Intel's 3D IC integration: chiplets, microbumps, RDLs, and Active TSV-interposer



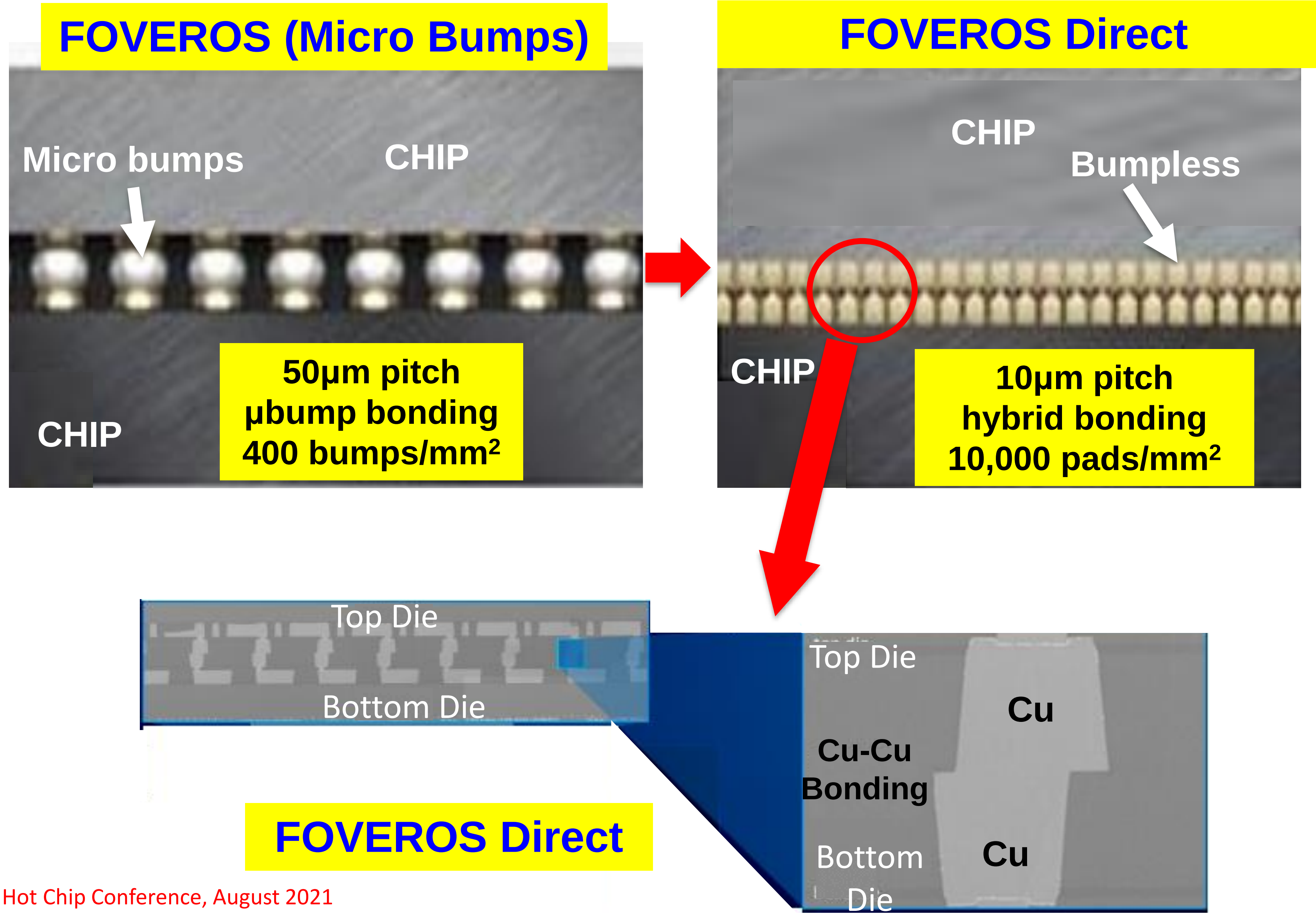






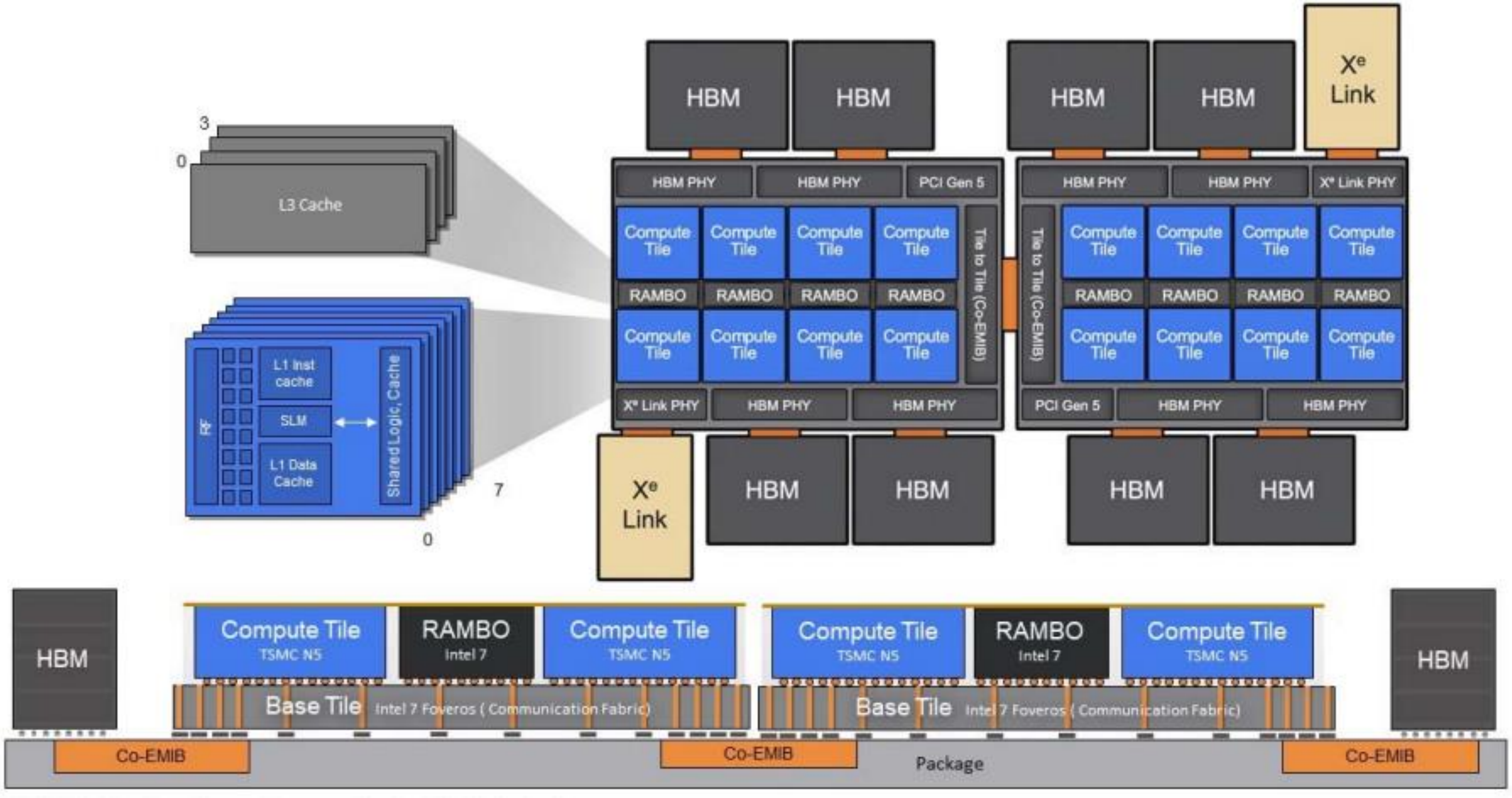
IEDM 2019 and ISSCC 2020

Intel's Future Chiplet Design and Heterogeneous Integration Packaging:- FOVEROS Direct

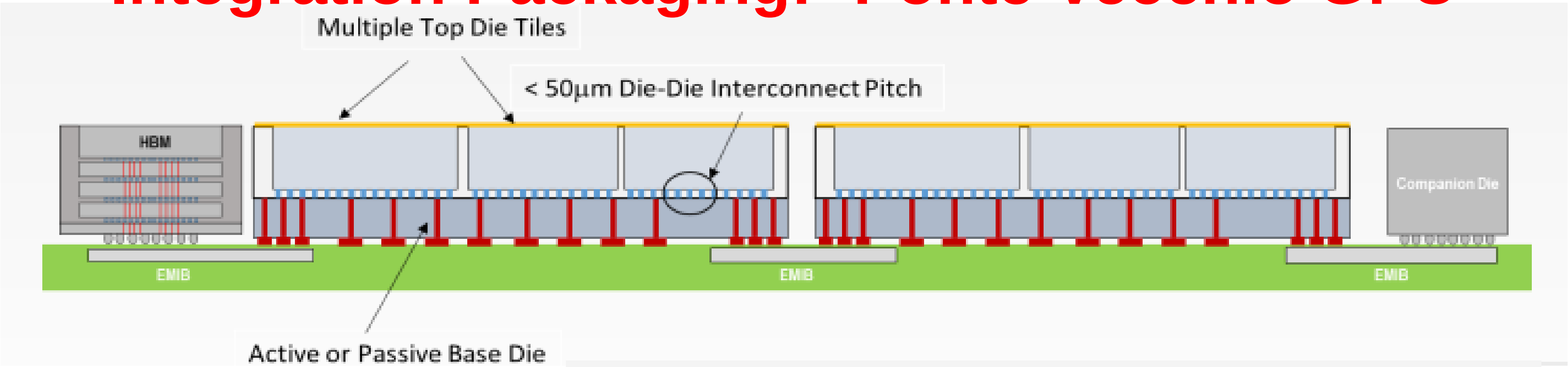


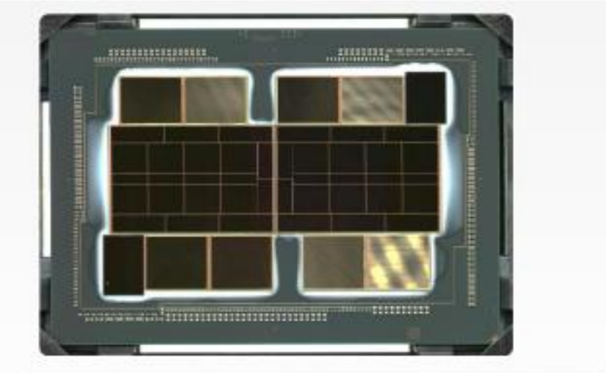
IEEE Hot Chip Conference, August 2021

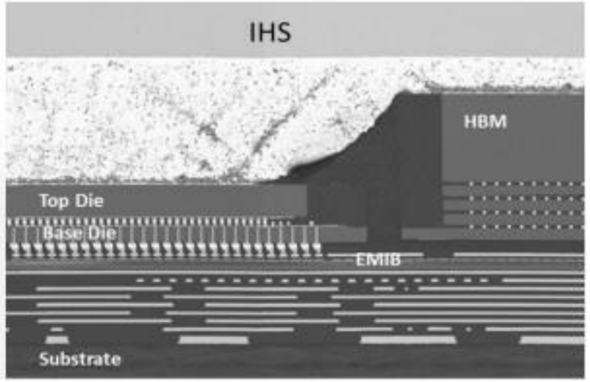
Intel's Future Chiplet Design and Heterogeneous Integration Packaging:- Ponte Vecchio GPU



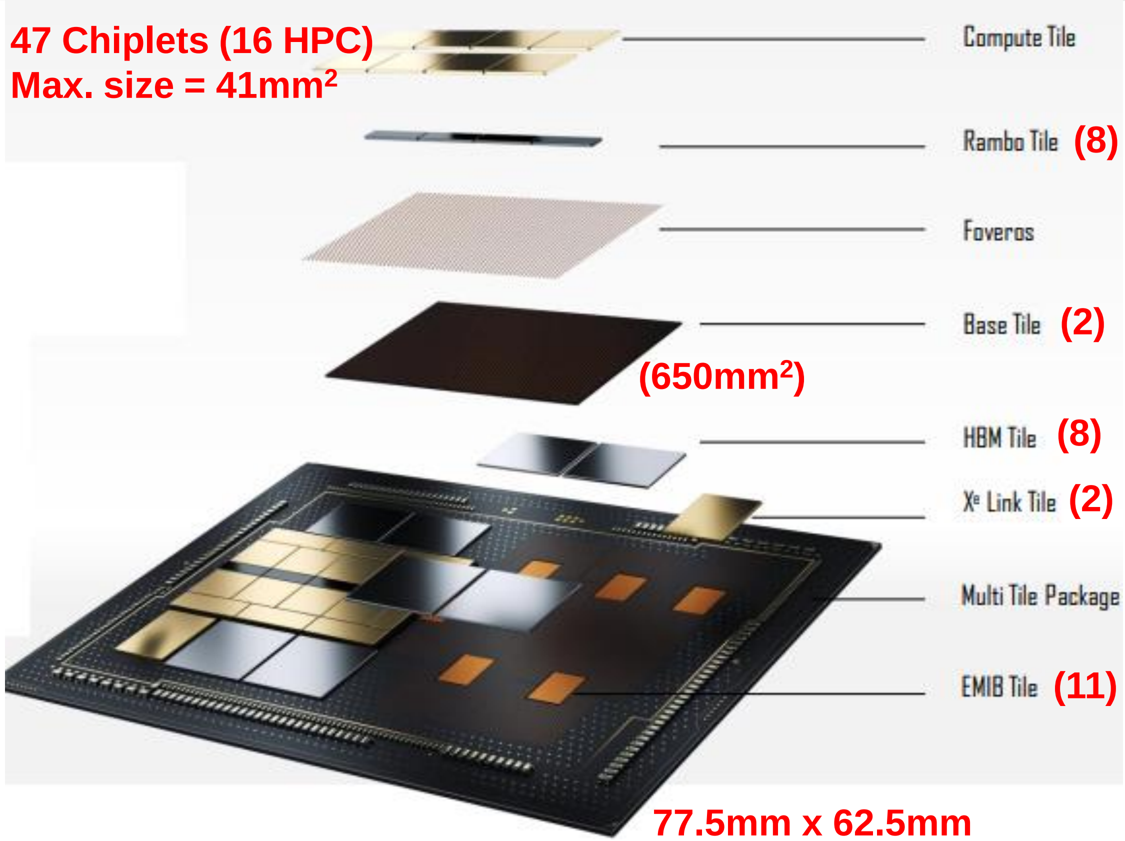
Intel's Future Chiplet Design and Heterogeneous Integration Packaging:- Ponte Vecchio GPU





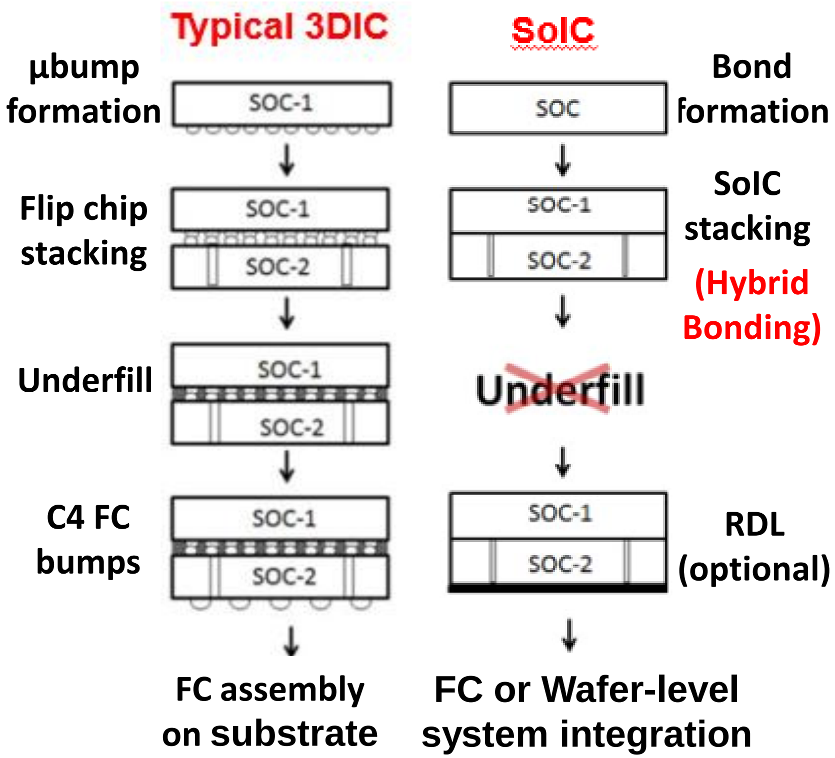


- 47 Chiplets (16 HPC)
- Max. size = 41mm^2

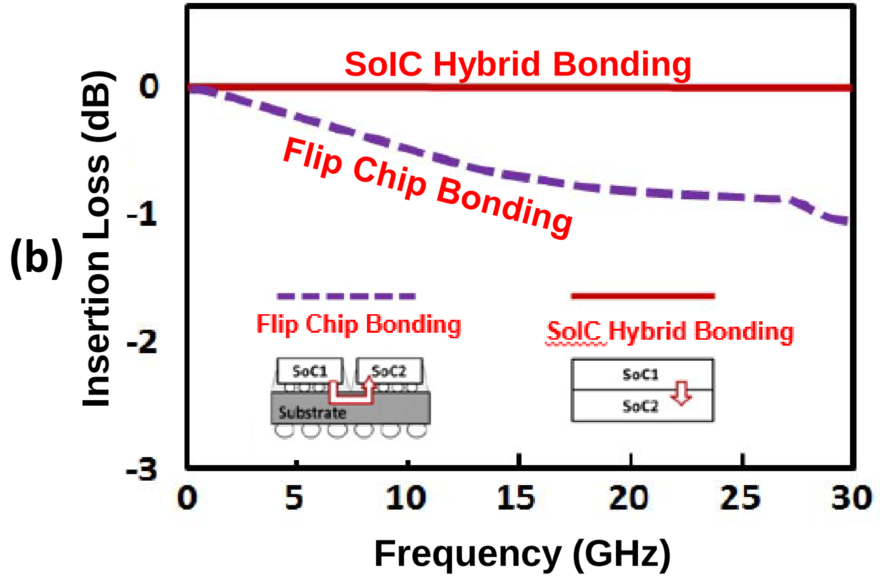


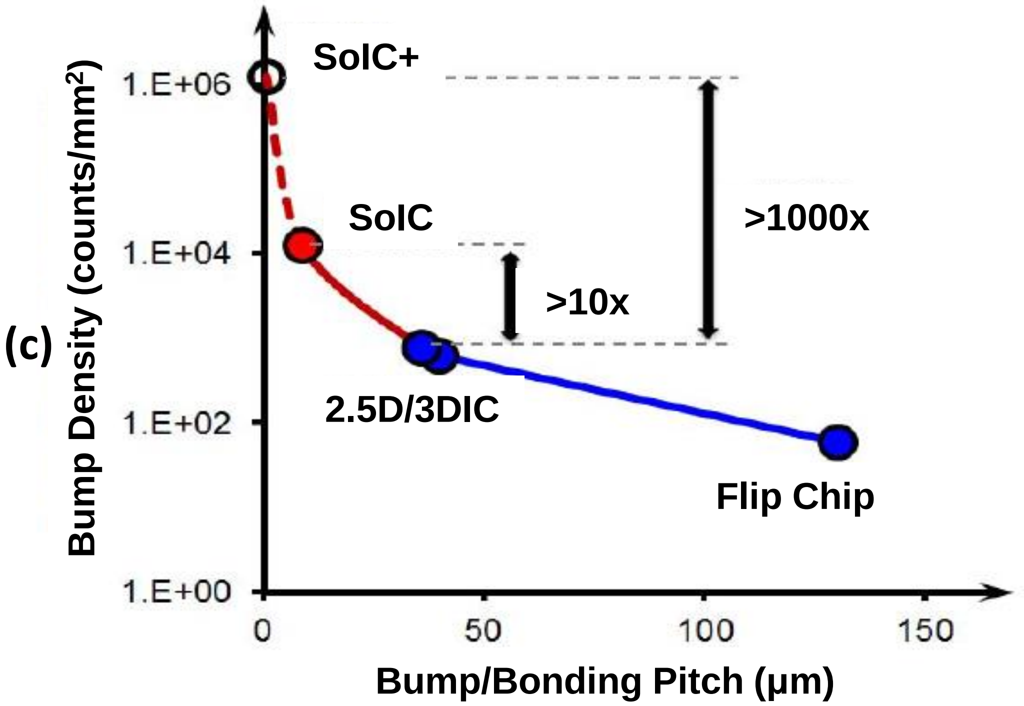
IEEE Hot Chip Conference, August 2021

TSMC's Chiplets Bonding, Density, and Performance



(a)

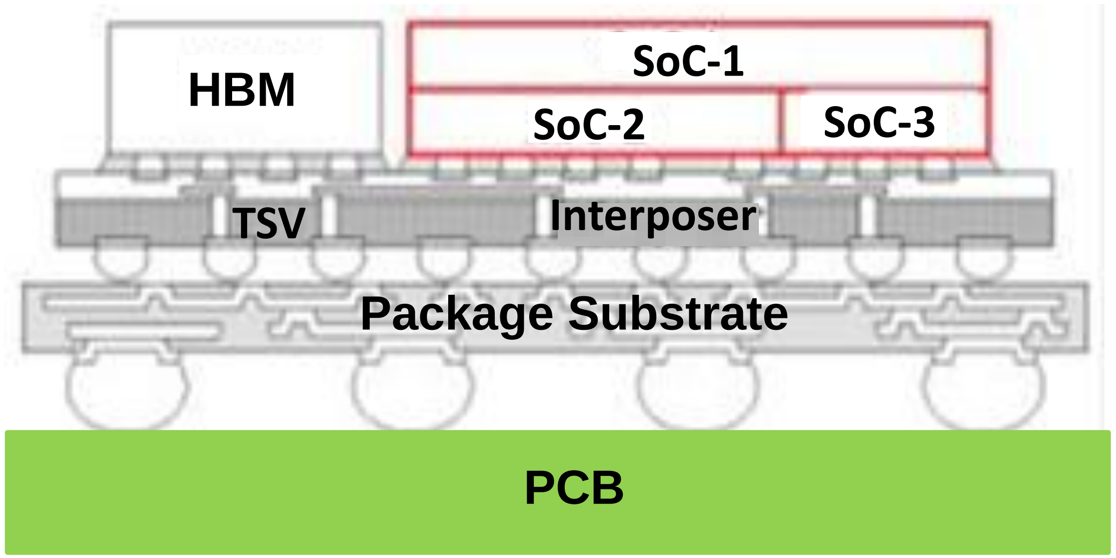




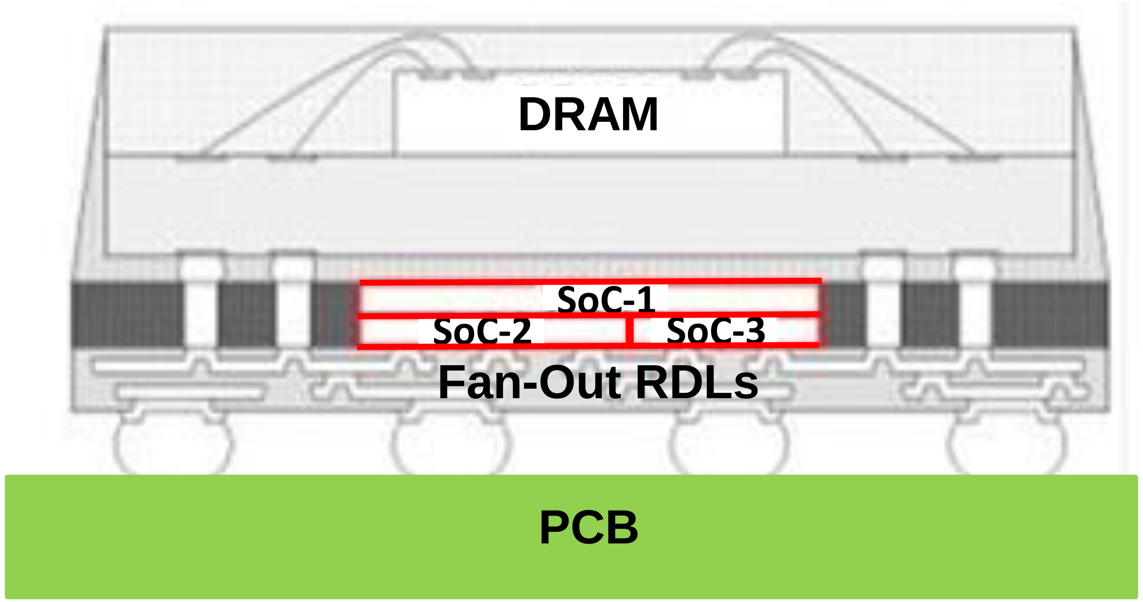
IEEE/ECTC2020 and 2021

TSMC's Chiplet Design and Heterogeneous Integration Packaging

CoWoS with SoIC

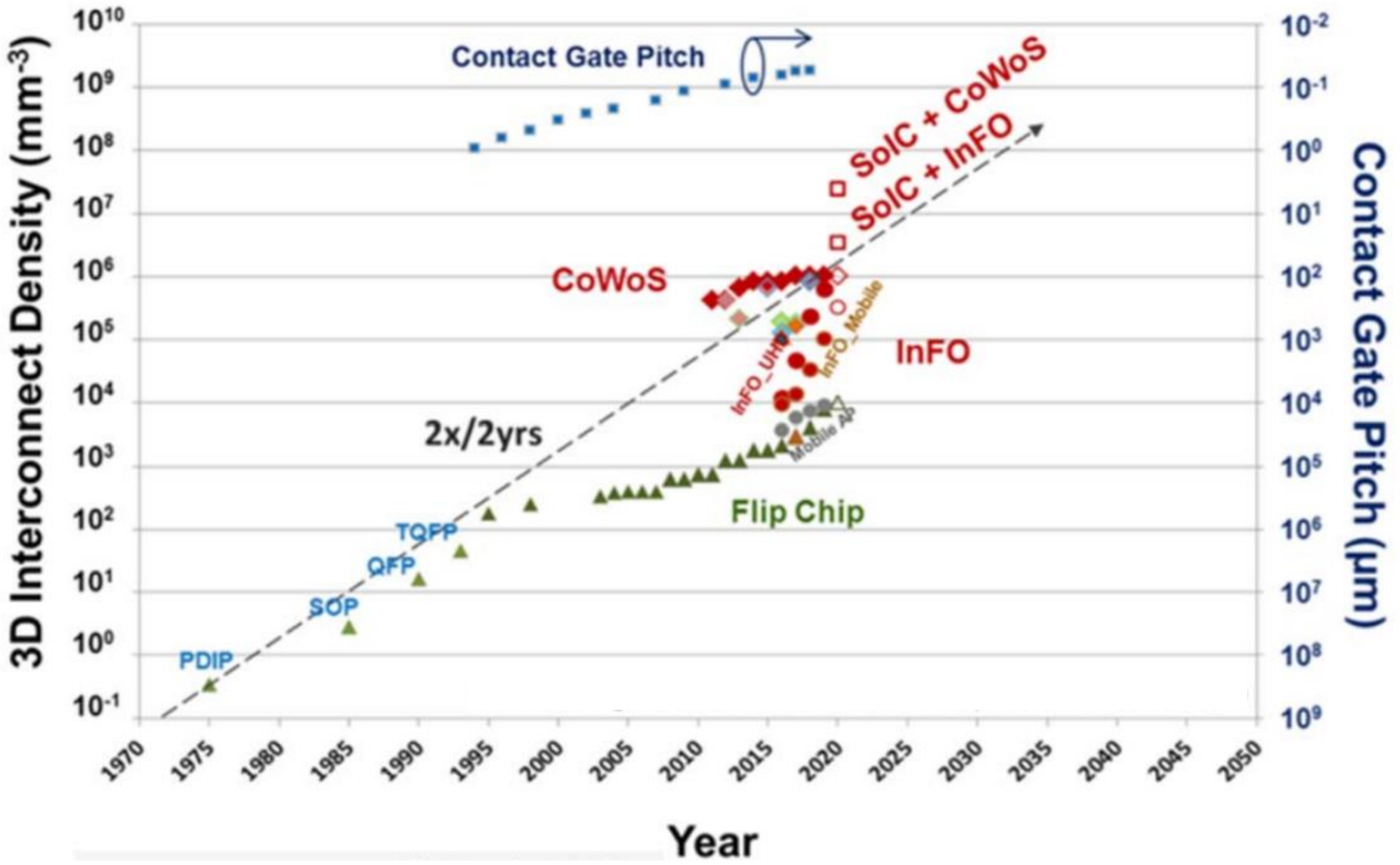


InFO PoP with SoIC



IEEE/ECTC2020 and 2021

TSMC's Chiplets Design and Heterogeneous Integration Packaging (SoIC + CoWoS and SoIC + InFO) Roadmap



IEEE/ECTC2020 and 2021

Lateral Communications (Bridges) between Chiplets

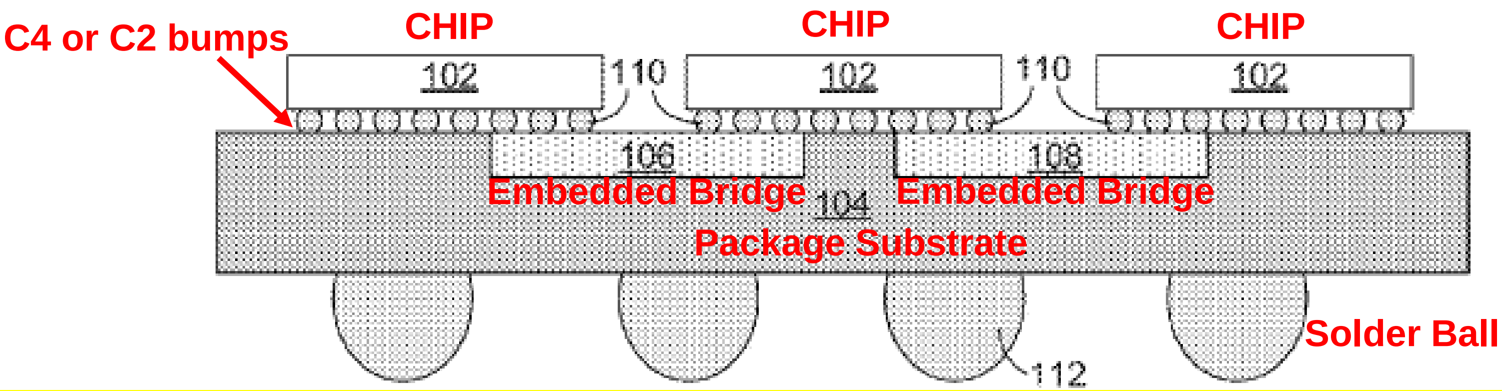
- **Bridge Embedded in Build-up Package Substrate**

- **Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)**

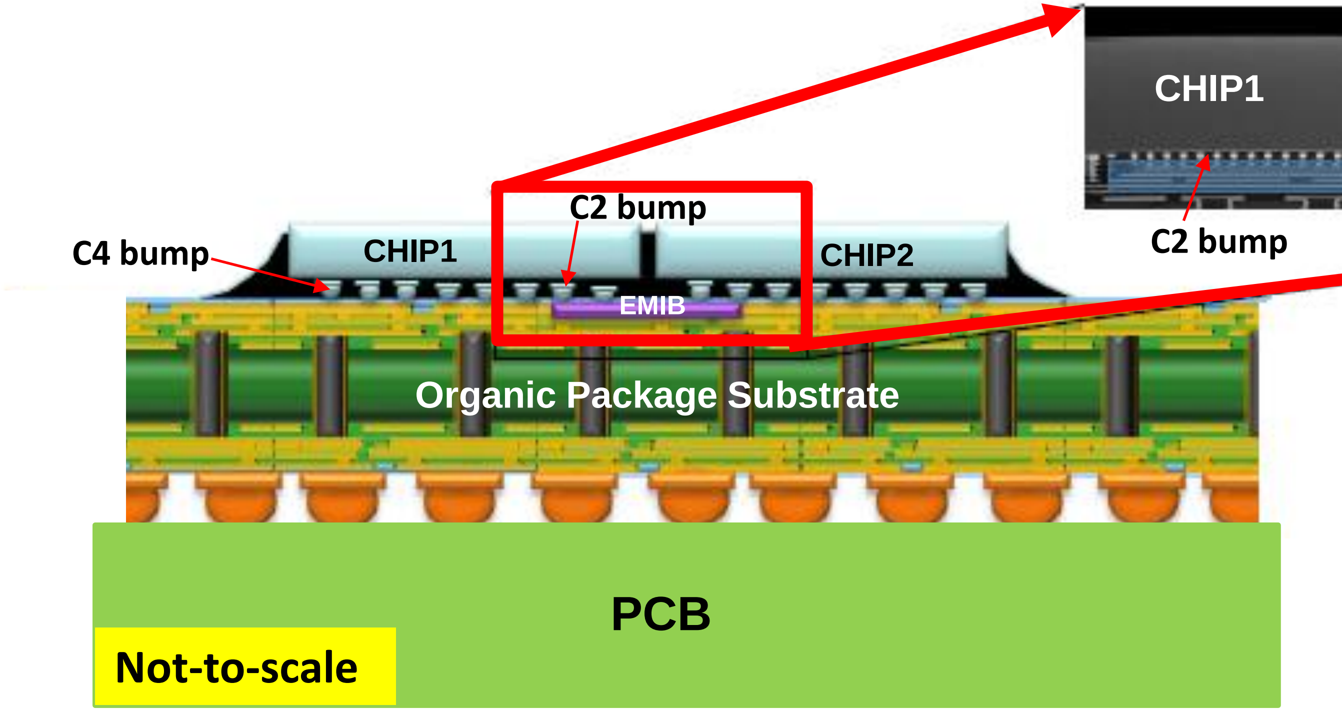
- **Hybrid Bridge**

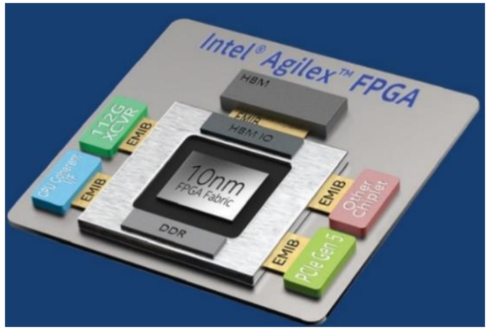
Bridge Embedded in Build-up Package Substrate

Intel's EMIB Patent and Agilex Module



Intel's Embedded Multi-die Interconnect Bridge (EMIB) in package substrate

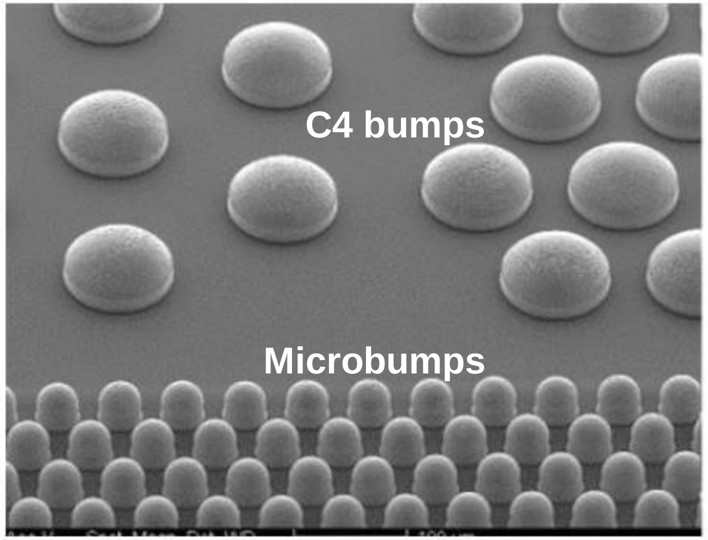


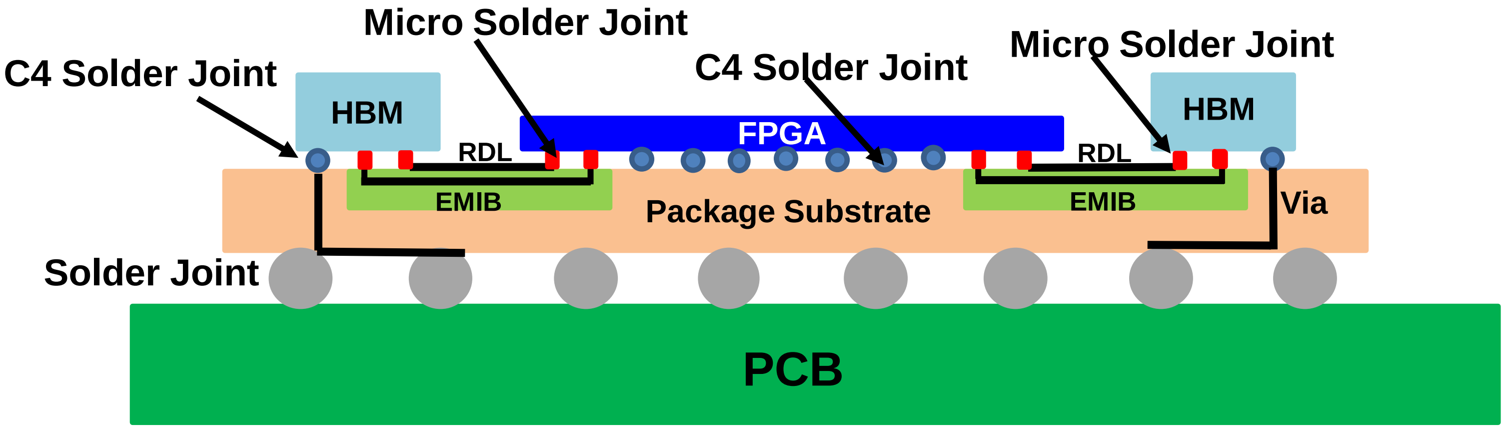


ECTC2016

Intel's FPGA (Agilex) with EMIB

FPGA

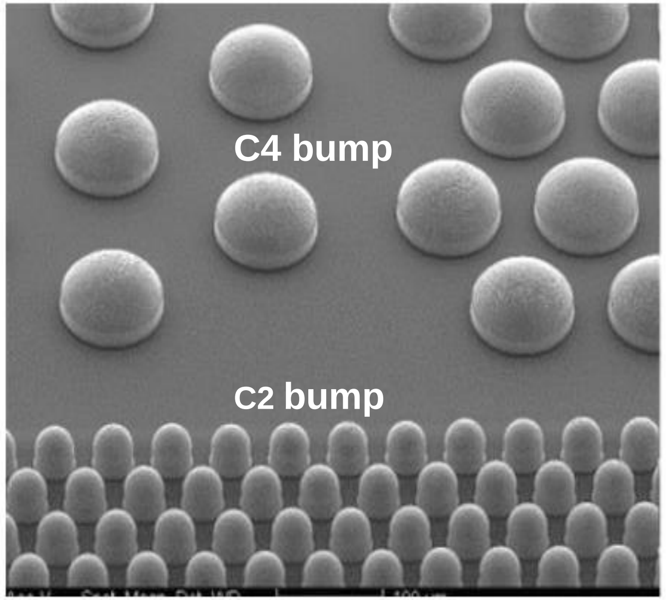




September 2019

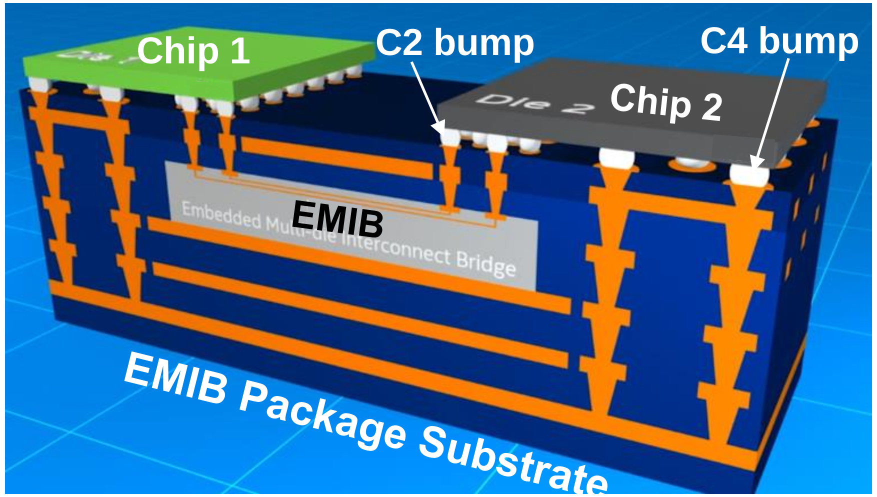
Intel's EMIB
(Embedded Multi-die Interconnect Bridge)

C4 (controlled collapse chip connection) bumps and C2 (Cu-pillar + solder cap) bump on chip

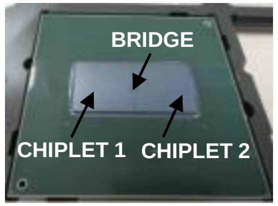


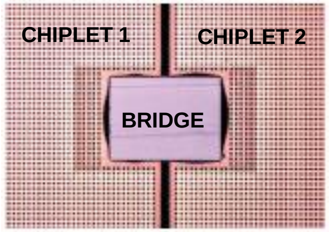
CHIP

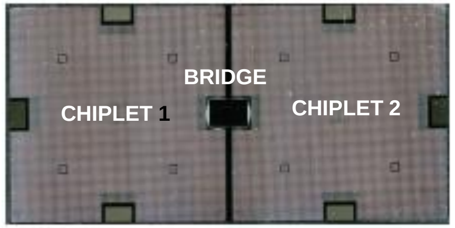
- The minimum metal L/S/H is 2μm.
- The dielectric layer thickness is 2μm.
- The bridge size is from 2mm x 2mm to 8mm x 8mm
- Usually, there are ≤ 4 RDLs.

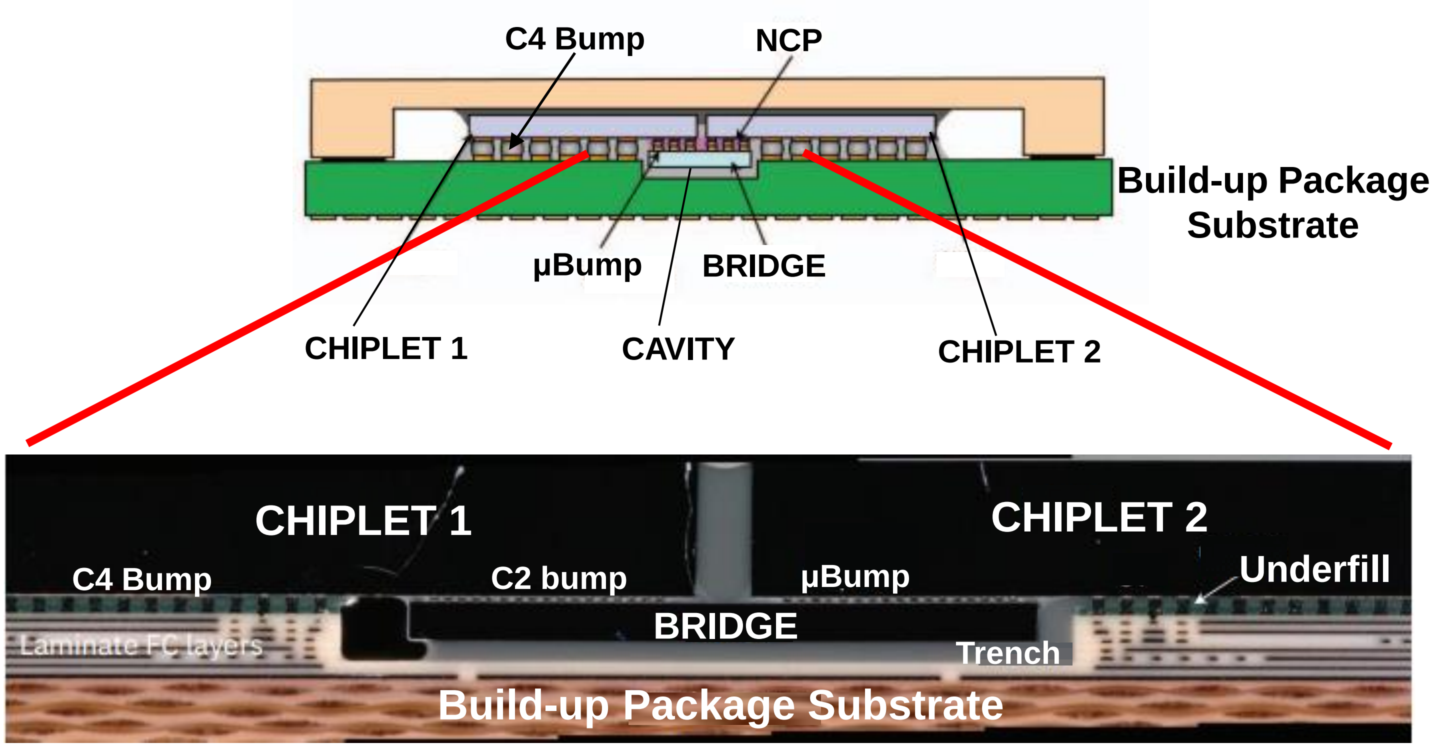


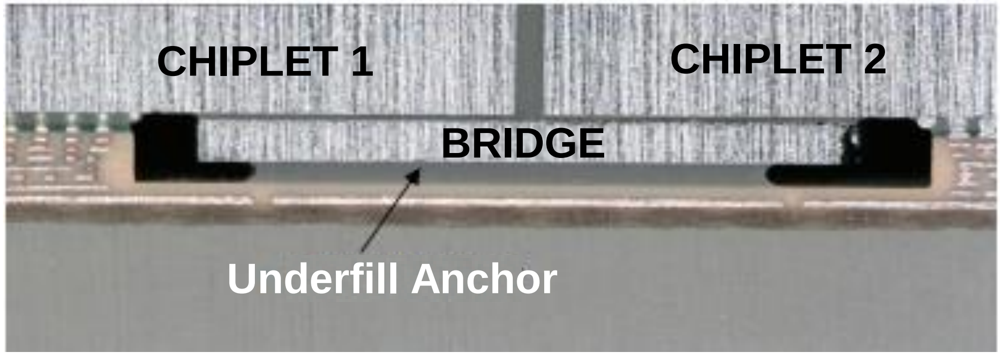
IBM's Direct Bonded Heterogeneous Integration (DBHi) Si Bridge

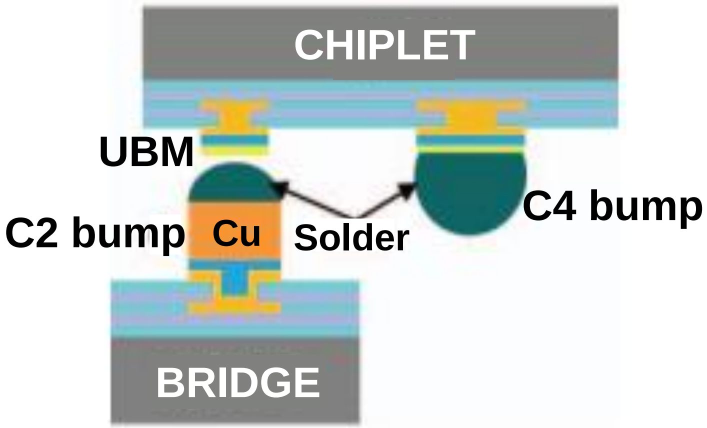








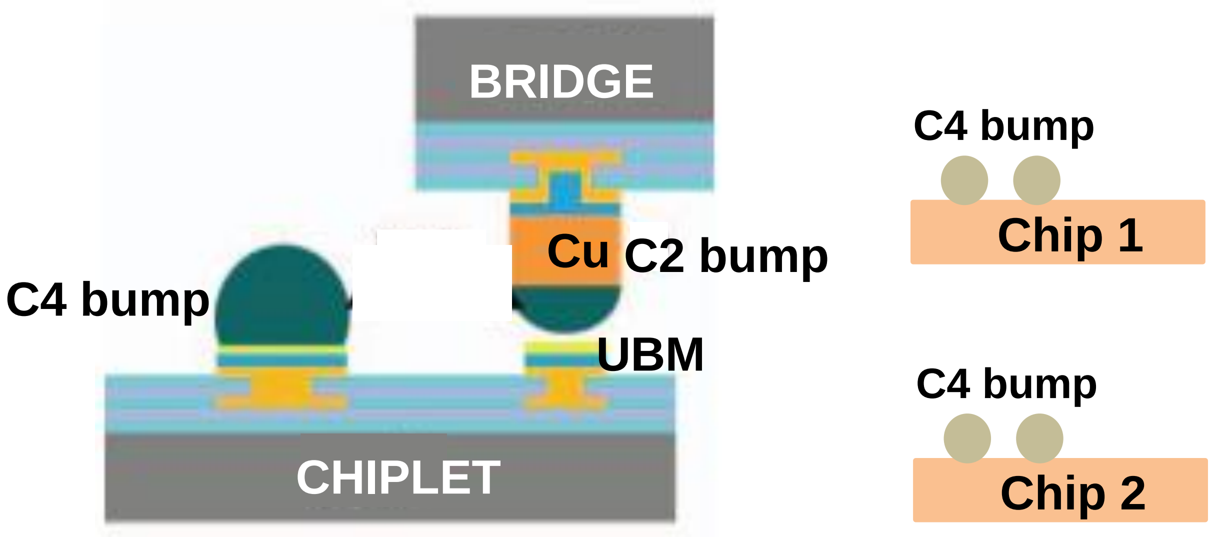




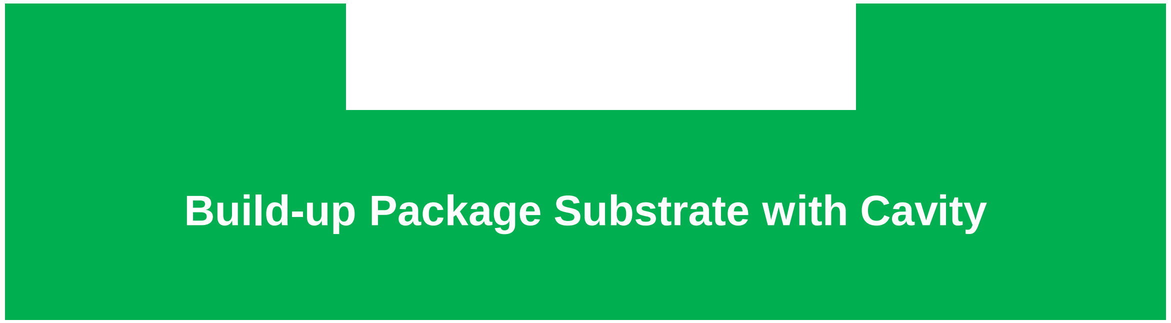
ECTC2021

IBM's DBHi Key Process Steps

(a)

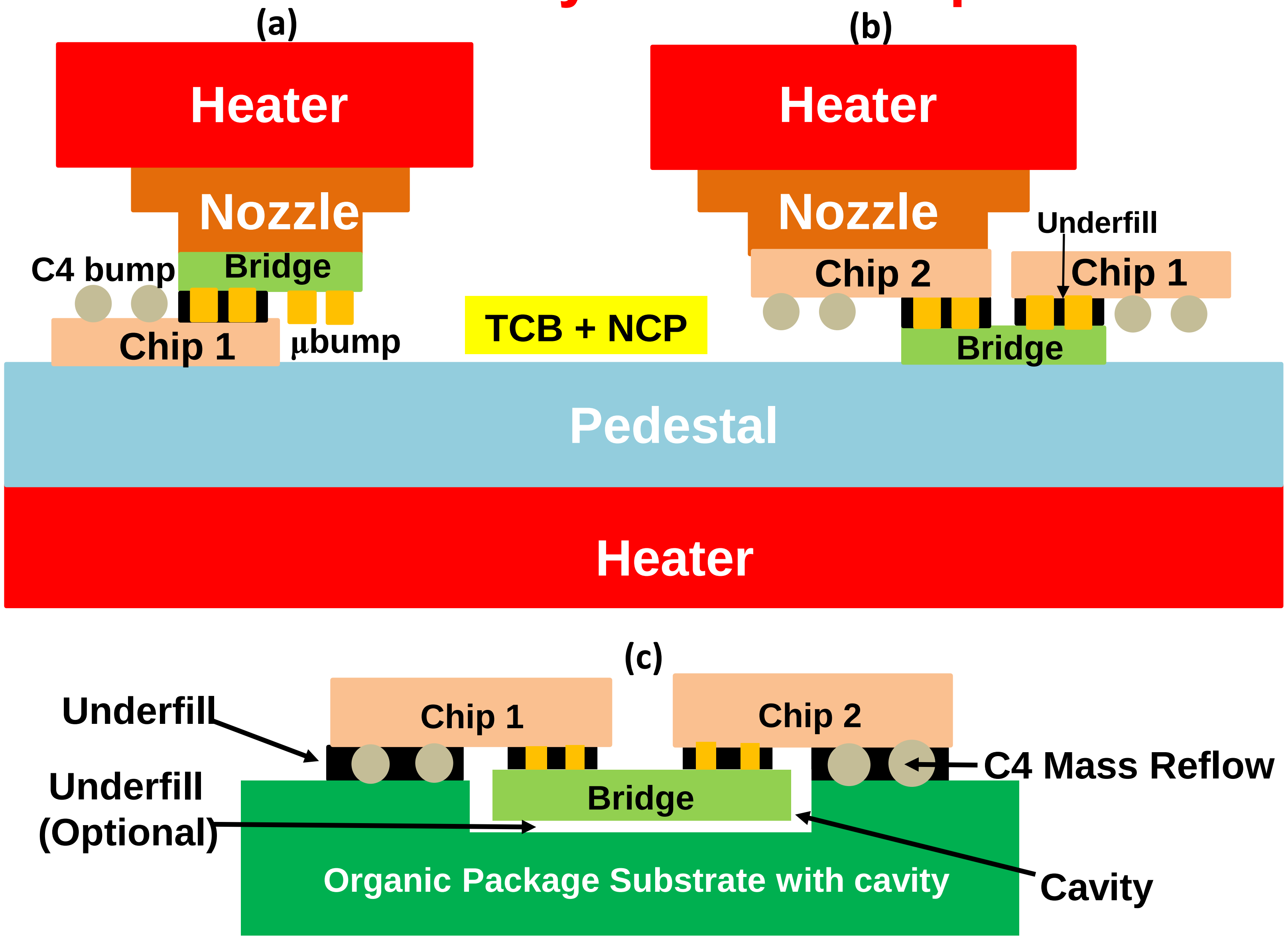


(b)



a) C2 bumps on the bridge, while C4 bumps on the chiplet.
b) Ordinary build-up package substrate with a cavity.

IBM's DBHi Key Process Steps

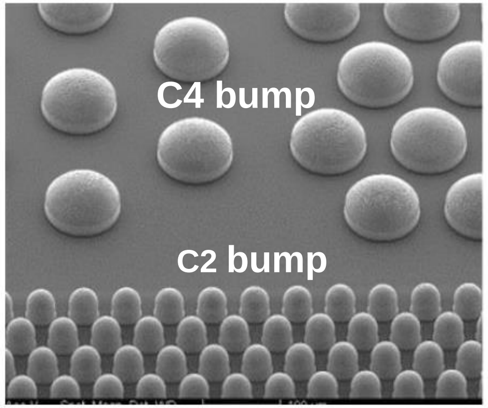


a) TCB/NCP of bridge die with C2 µbumps on Chip 1 with C4 bumps (NCP becomes the underfill).
b) TCB/NCP of Chip 2 with C2 µbumps on the bridge with the bonded Chip 1.
c) Place the module (bridge + Chip 1 + Chip 2) on the substrate and mass reflow the C4 bumps. Apply the capillary underfill to the C4 bumps.

Differences between Intel's EMIB and IBM's DBHi

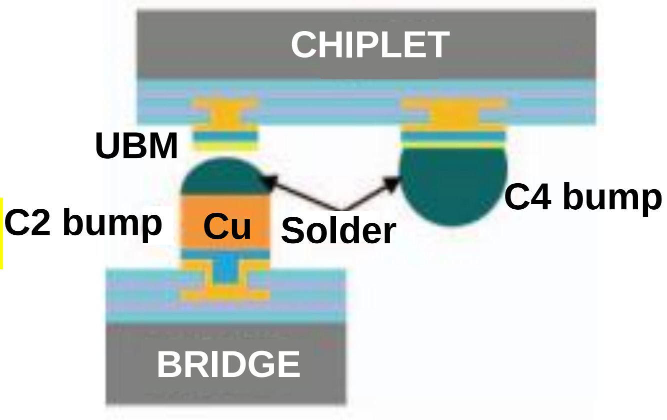
- For Intel's EMIB, there are two different (C4 and C2) bumps on the chiplets (and there are no bumps on the bridge), while for IBM's DBHi, there are C4 bumps on the chiplets and C2 bumps on the bridge.

EMIB



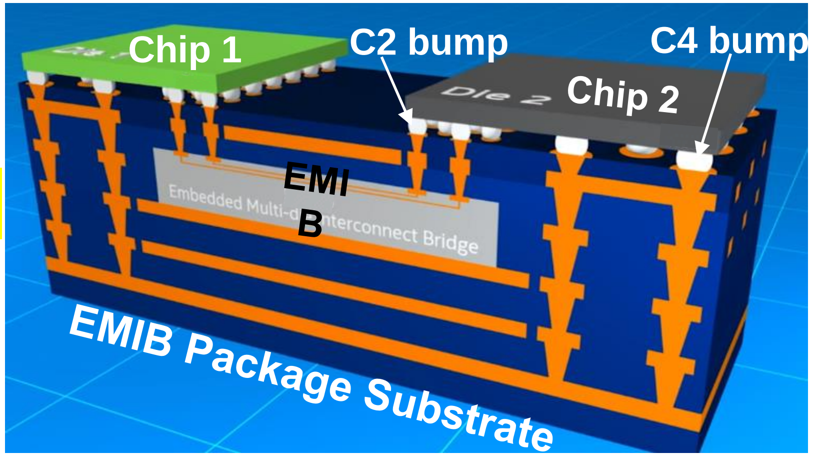
CHIPLET

DBHi



- For Intel's EMIB, the bridge is embedded in the cavity of a build-up substrate with a die-attach material and then laminated with another build-up layer on top. Therefore, the substrate fabrication is very complicated. For IBM's DBHi, the substrate is just a regular build-up substrate with a cavity on top.

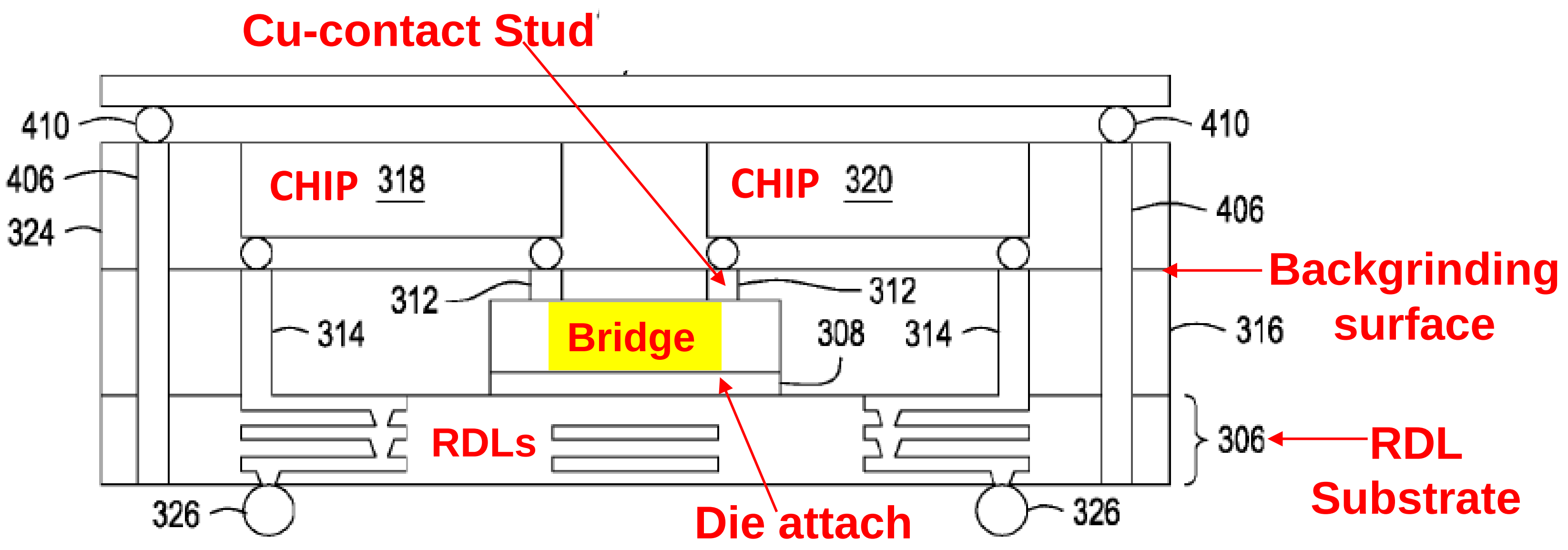
EMIB



DBHi

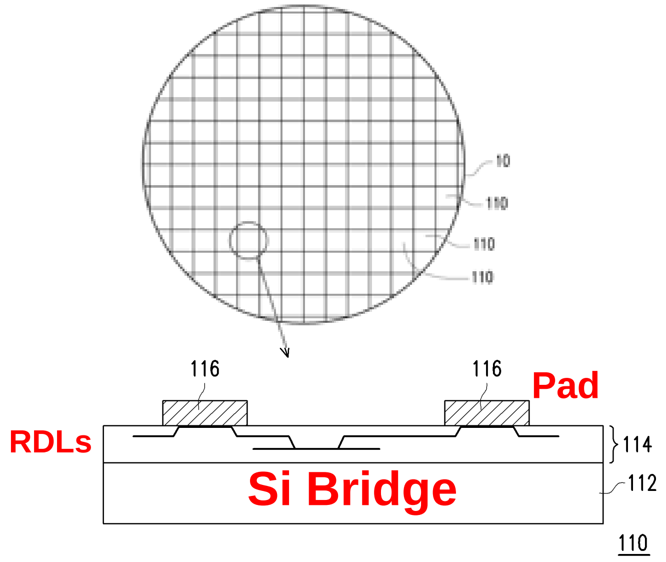
Bridge Embedded in Fan-Out Epoxy Molding Compound (EMC)

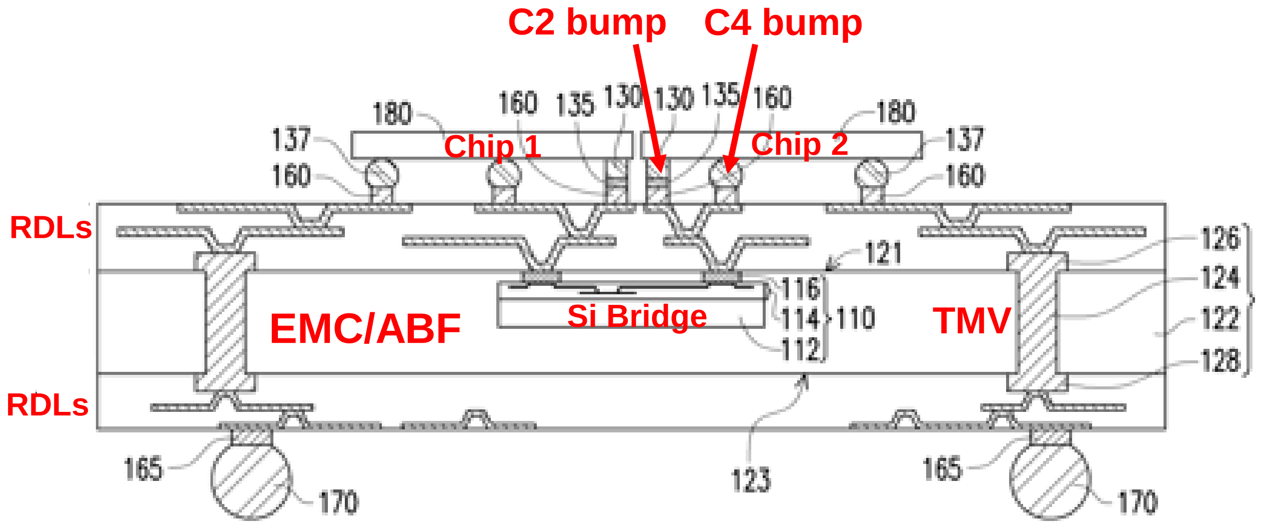
Applied Materials' Fan-out Chip (Bridge) First Face-up Process



US patent 10,651,126 (filed on December 8, 2017)

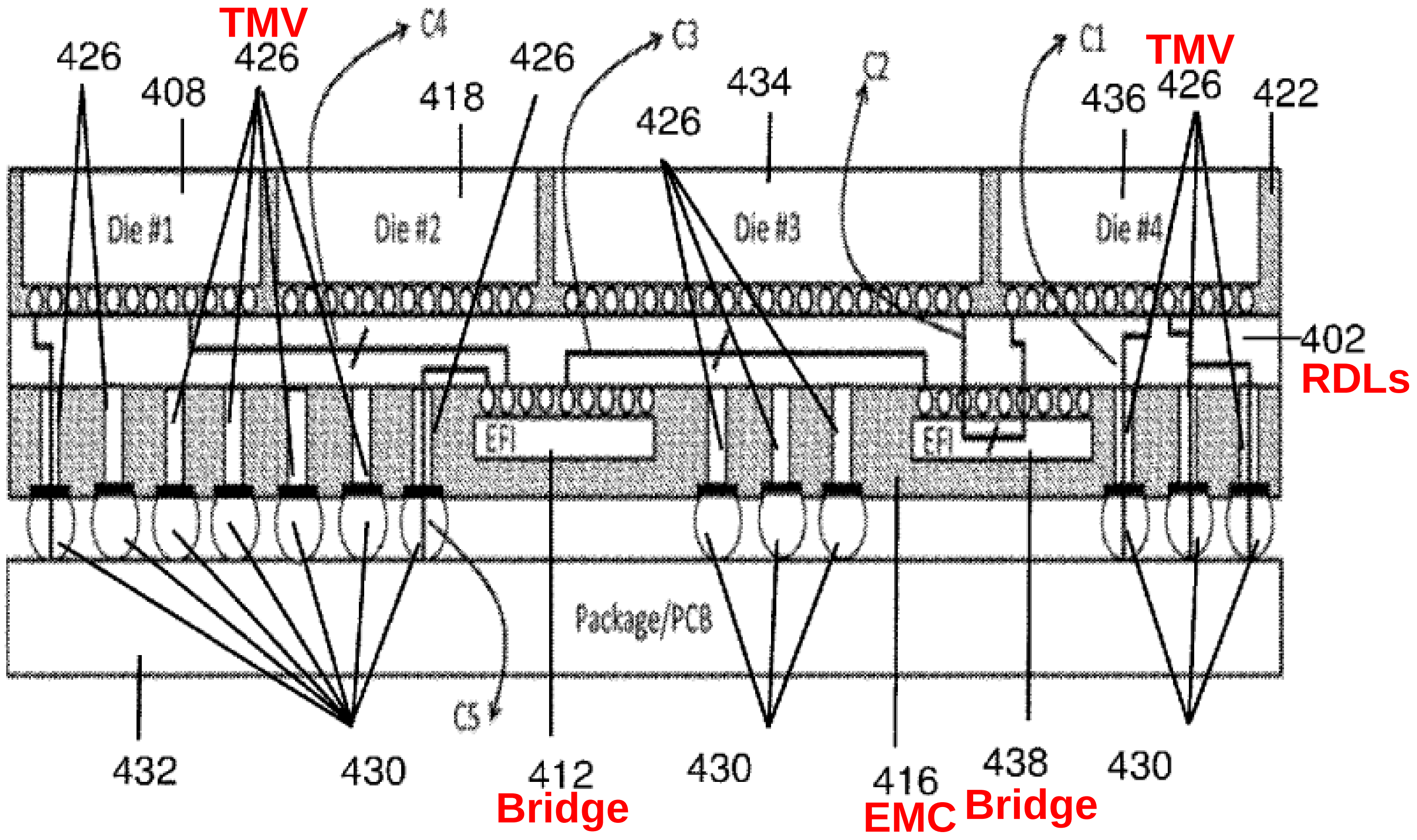
Unimicron's Fan-out Chip (Bridge) First Face-down Process





U.S. patent 11,410,933, patent date: Aug. 9, 2022.

IME's Fan-out Chip (Bridge) Last (RDL – First) Process

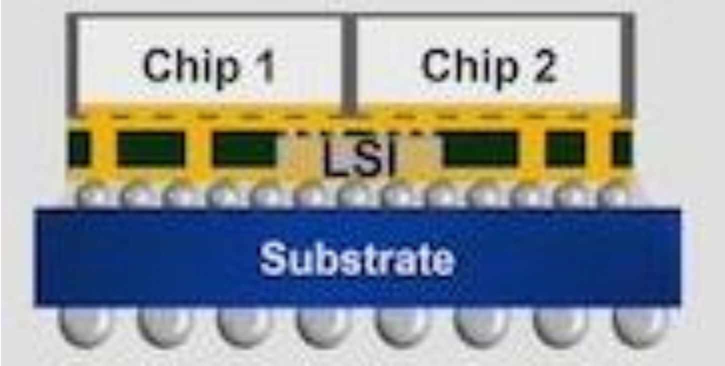


US 11,018,080 (May 25, 2021)

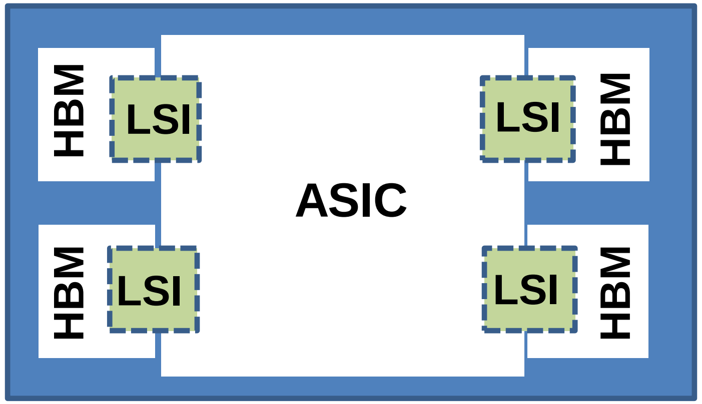
TSMC's LSI (Local Silicon Interconnect)

Fan-out Chip (Bridge) First Face-up Process

InFO_LSI



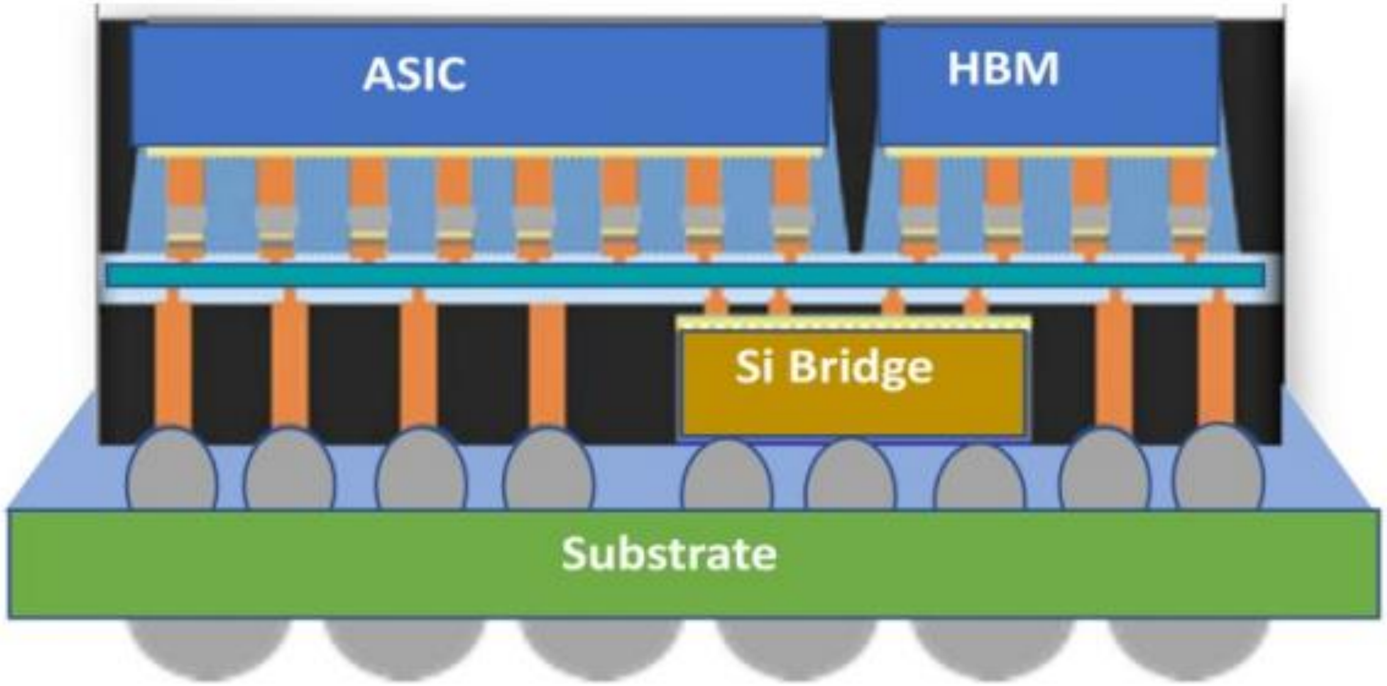
CoWoS_LSI



TSMC Annual Technology Symposium, August 25, 2020

Advanced HDFO Packaging Solutions for Chiplets Integration in HPC Application

Lihong Cao Teck Lee1 , Yungshun Chang1 , SimonYL Huang1 , JY On1 , Emmal Lin1 and Owen Yang1
Advanced Semiconductor Engineering Inc. (US) Inc., Austin, TX 78704. USA 1 Corporate R&D Center, Advanced Semiconductor Engineering Inc., Kaohsiung, Taiwan (R.O.C)

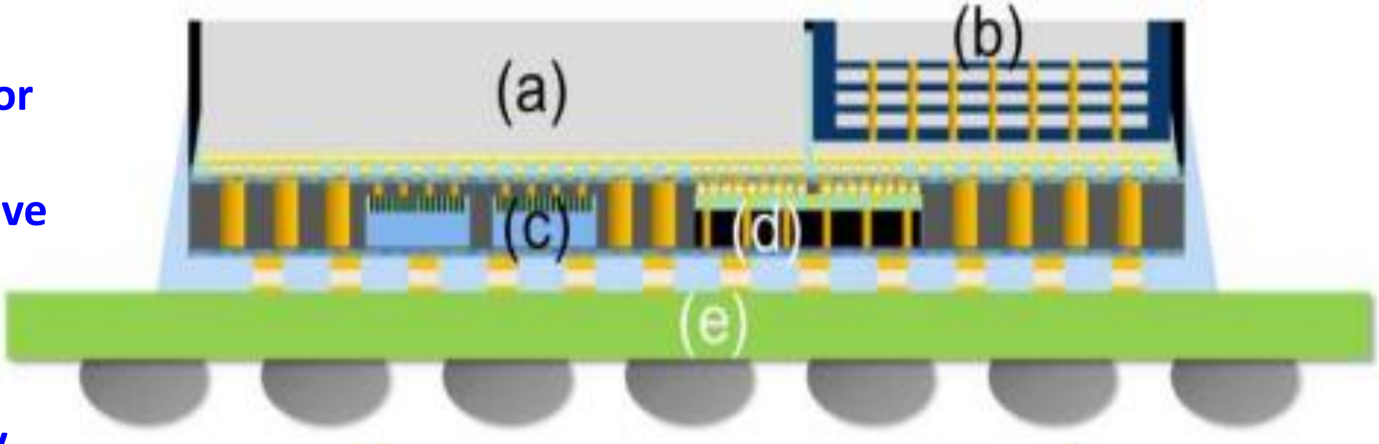


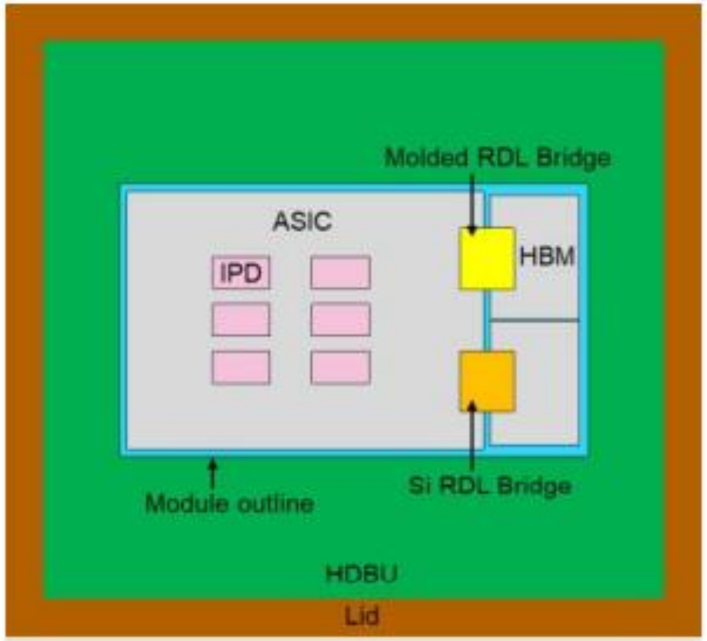
sFOCoS (Stacked Si bridge Fan-Out Chip-on-Substrate)

S-Connect Fan-out Interposer For Next Gen Heterogeneous Integration

JiHun Lee, GamHan Yong, MinSu Jeong, JongHyun Jeon, DongHoon Han, MinKeon Lee , WonChul Do, EunSook Sohn, Mike Kelly, Dave Hiner JinYoung Khim
Research & Development Amkor Technology Korea Incheon, Korea JinYoung.Khim@amkor.co.k

(a) ASIC or processor
(b) HBM
(c) integrated passive device or active device
(d) bridge die for ASIC to memory interconnection
(e) Package substrate





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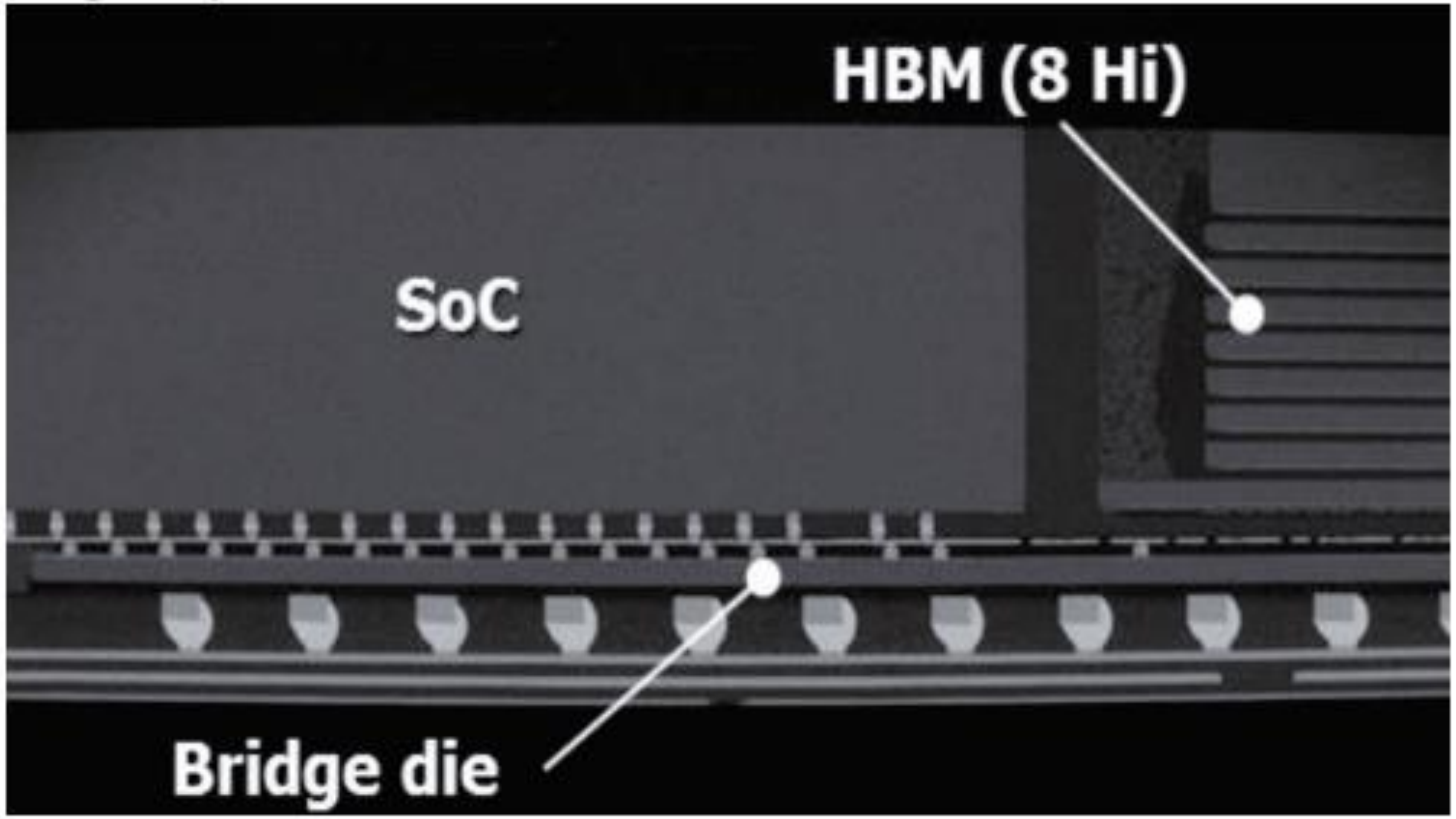
Electrical Performances of Fan-Out Embedded Bridge (FO-EB)

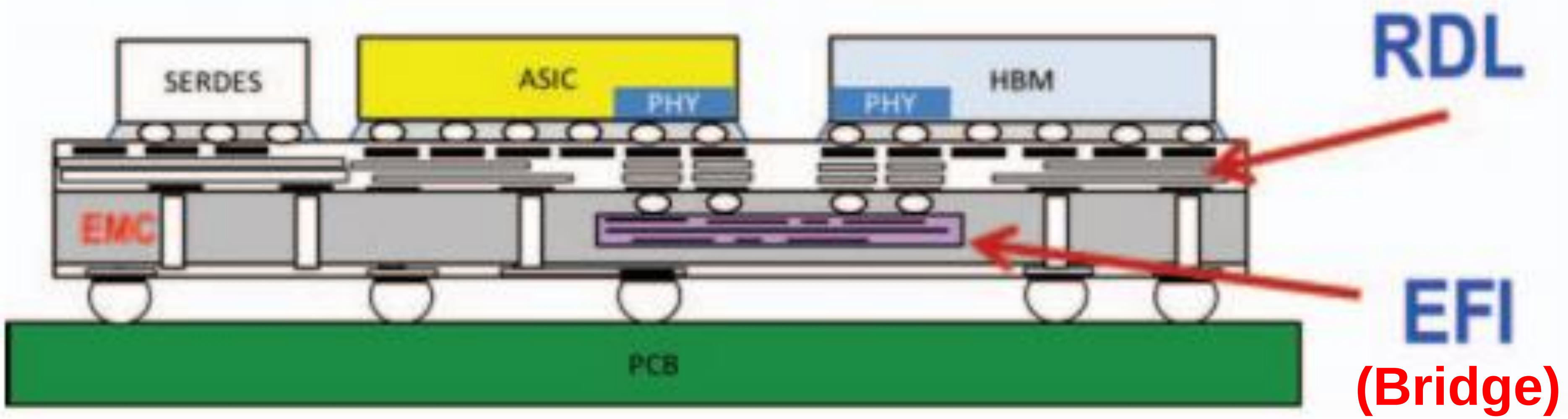
JinWei You, Jay Li, David Ho, Jackson Li, Ming Han Zhuang, David Lai, C. Key Chung, Yu-Po Wang
Siliconware Precision Industries Co. Ltd Taichung, Taiwan jinweiyou@spil.com.tw



IEEE/ECTC2021

Heterogeneous Integration with Embedded Fine Interconnect (EFI)

Chai Tai Chong, Lim Teck Guan, David Ho, Han Yong, Chong Ser Choong, Sharon Lim Pei Siang, Surya Bhattacharya Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research) 2 Fusionopolis Way, #08-02 Innovis Tower, Singapore 138634 chaitac@ime.a-star.edu.sg, +65-6770-5425



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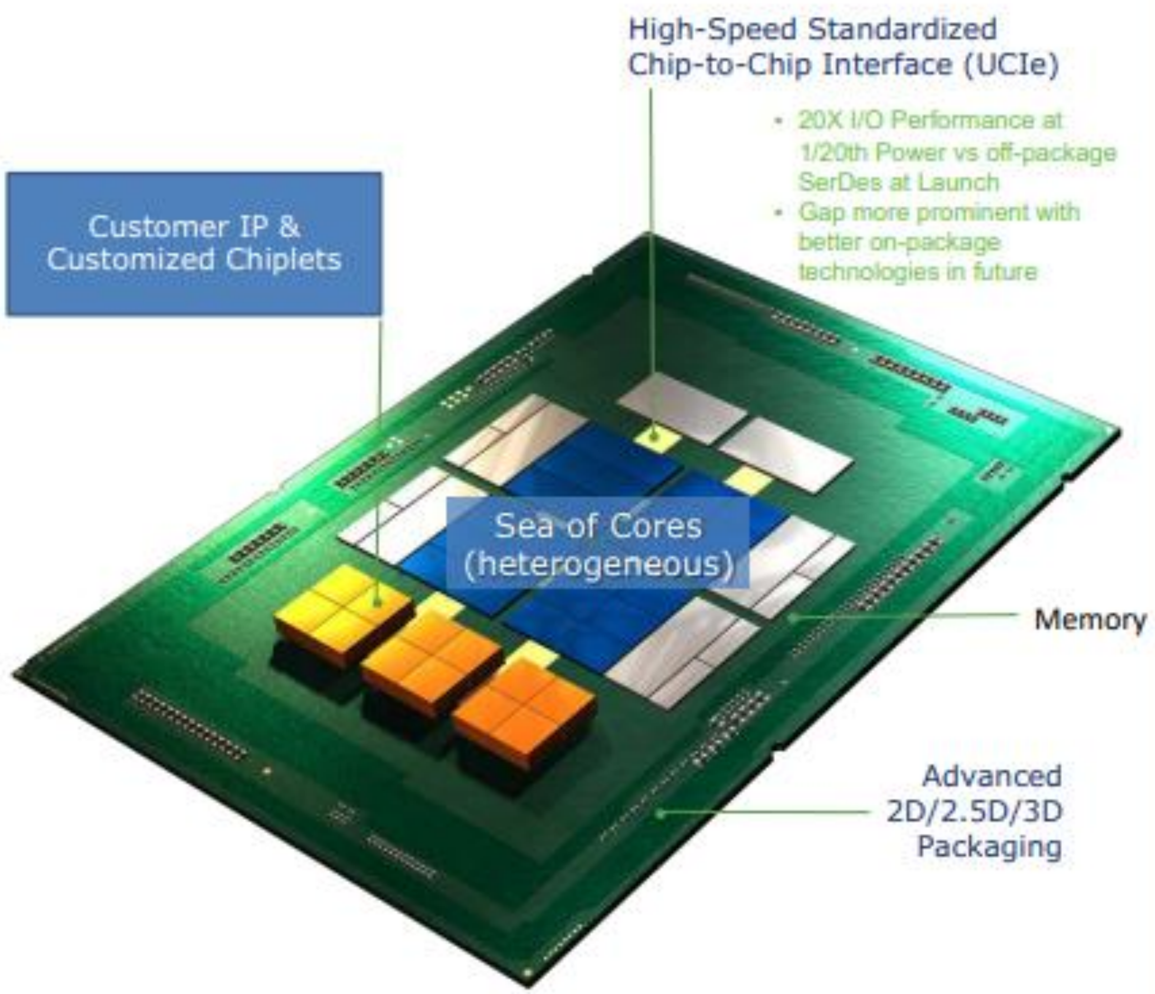
Motivation

OPEN CHIPLET: PLATFORM ON A PACKAGE



Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing and process locked IPs)

PROMOTERS

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive a new open chiplet ecosystem.

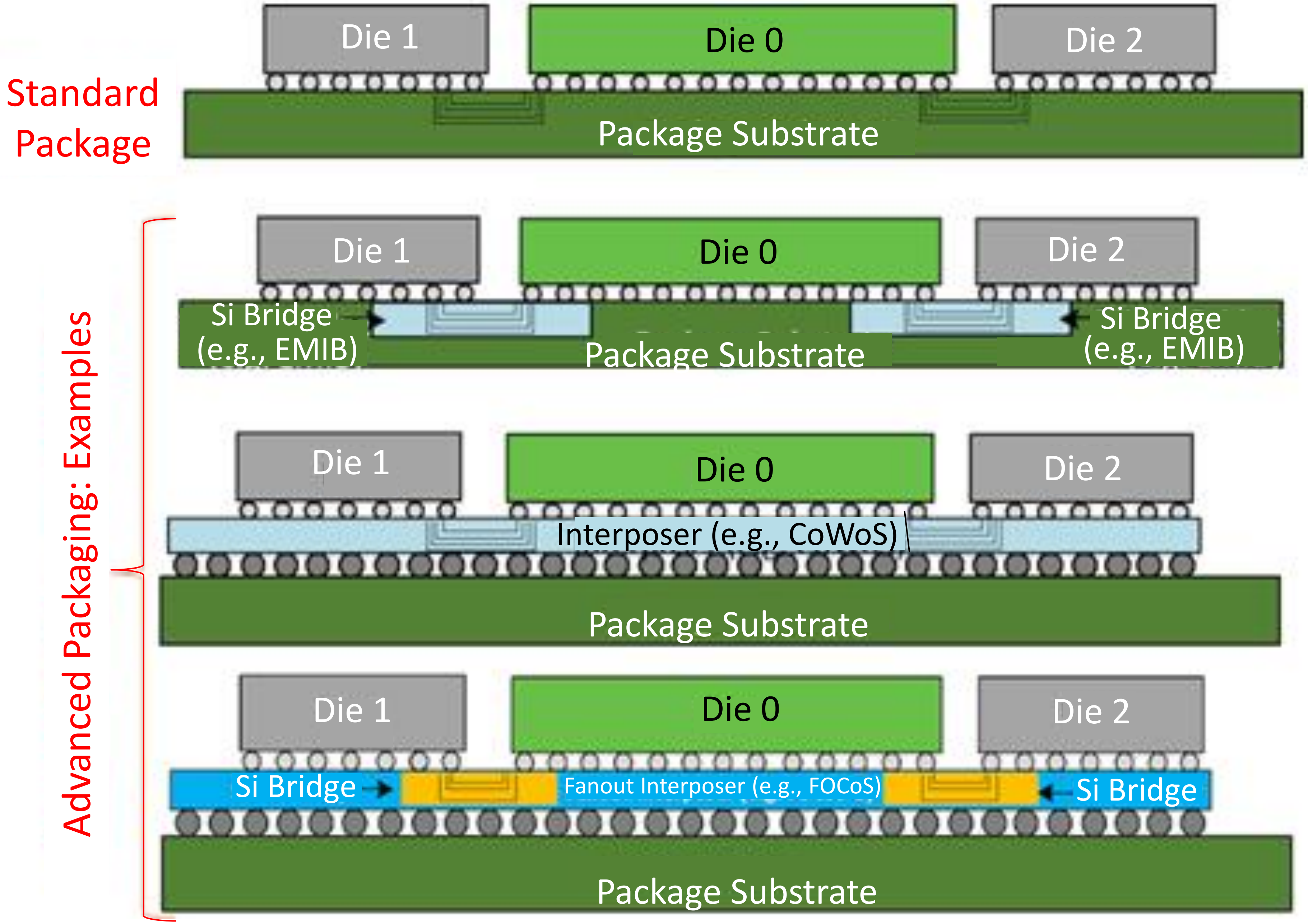
AMD arm ASE GROUP

Google Cloud intel. Meta

Microsoft Qualcomm SAMSUNG tsmc

Alibaba Group NVIDIA.

Different flavors of packaging options supported to build an open ecosystem



UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years. Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.

UCIe Universal Chiplet Interconnect Express

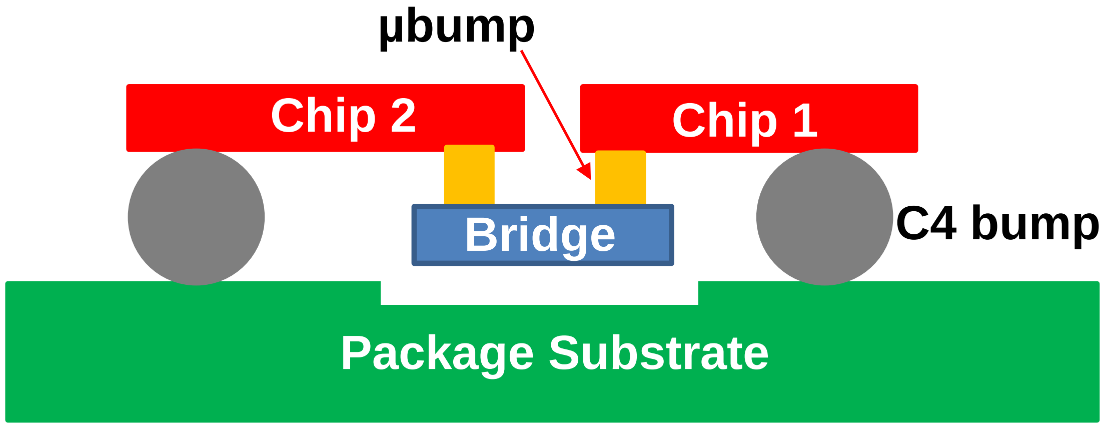
UCIe 1.0: Characteristics and Key Metrics

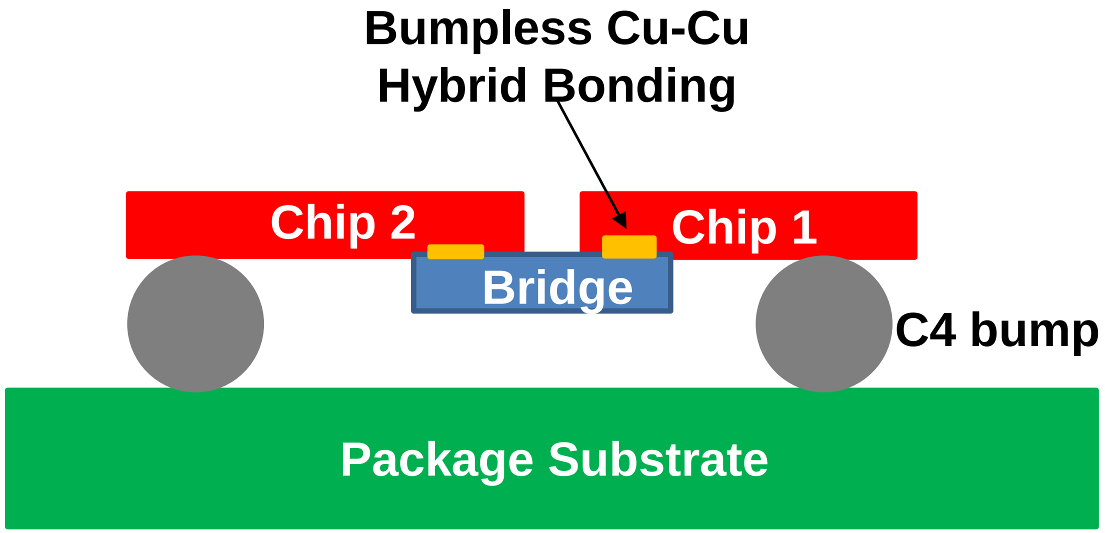
CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

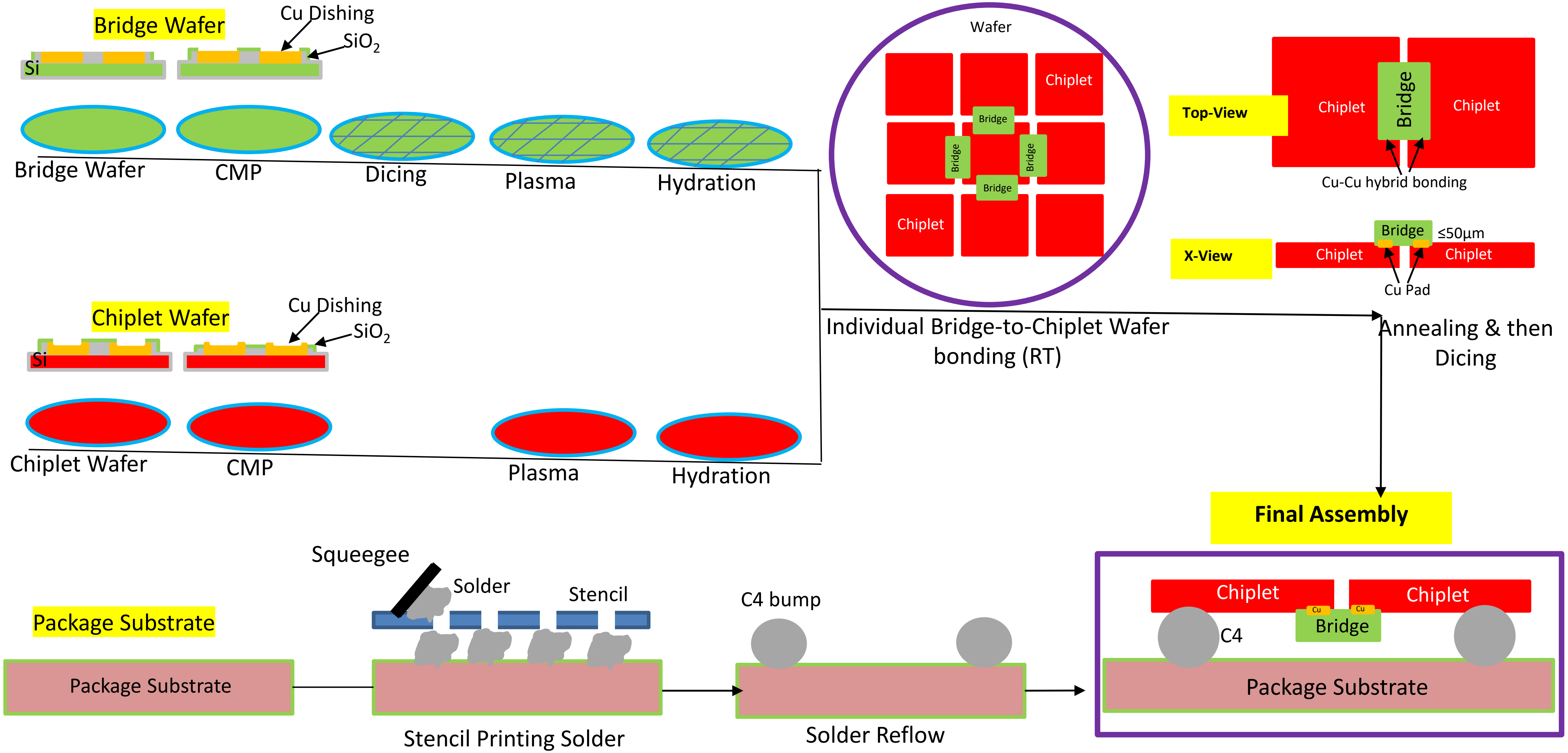
Hybrid Bonding Bridge

Hybrid Bonding Bridge

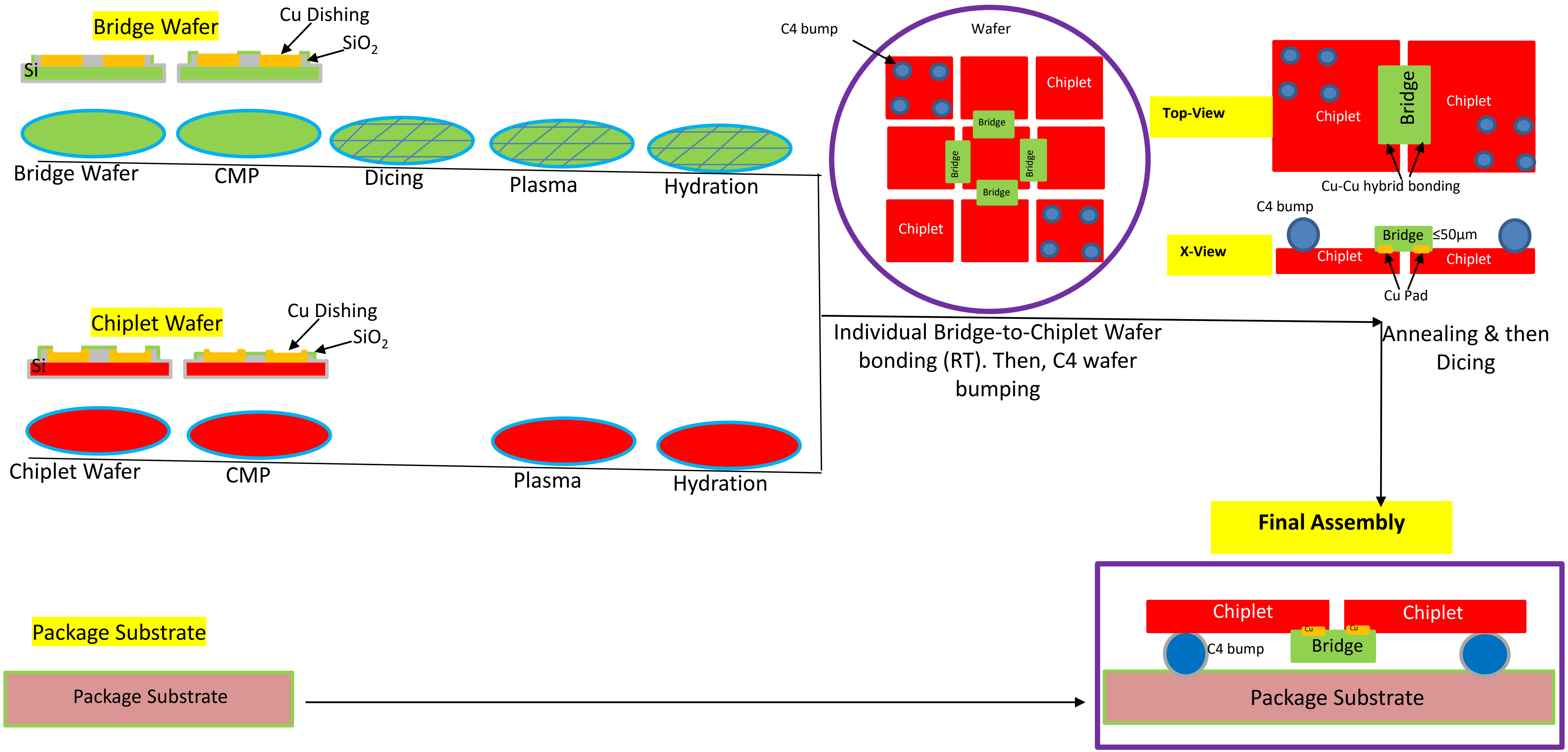




Bridge Wafer, Chiplet Wafer, and Package Substrate Process Flow (Option One)



Bridge Wafer, Chiplet Wafer, and Package Substrate Process Flow (Option Two)



Thank You Very Much for Your Attention!

☺