El Capítulo Guadalajara de la Sociedad de Teoría y Técnicas de Microondas (MTT-S) del IEEE invitan cordialmente a la conferencia magistral:

Achieving High Quality IO IP in Advanced Process Nodes: Challenges and Solutions by Intel Principal Engineer Daudi Onsongo

SYNOPSIS

We are in the age of ubiquitous compute – from hand-held devices to the cloud. This drives demand for high-speed data transfer between and within the microchips that are in the systems that define this distributed compute infrastructure. Input/Output IPs that enable this data transfer are implemented using a mixture of both digital and analog circuitry. Over the past few decades, we have seen continued acceleration in bandwidth requirements for Input/Output (IO) IP that support these high data transfer rates. At the same time Silicon Technology nodes continue to scale to provide the performance required for compute. This scaling is particularly challenging for analog circuitry which is sensitive to process variation. The combination of technology scaling and increasing bandwidth requirements has driven acceleration of complexity in IO Design and dependence on firmware for training and calibration. In this presentation the author will review Technology Scaling and its impact on analog circuit design and implementation. He will talk about the challenges he has observed in ensuring the delivery of high-quality IO IPs in these advanced nodes. Finally, he will propose some solutions and future directions he believes necessary to overcome these challenges.

Daudi Onsongo joined Intel in July of 2018 as a Principal Engineer in Analog Test and Validation. He has over 20 years of experience in technical disciplines spanning Semiconductor Process Technology Development, IC Design and Silicon Validation. He thrives in the intersection of design and process technology – and has built a career around it. Daudi received his B.S.E.E, M.S. and Ph.D. from the University of Texas at Austin in 1996, 2000 and 2003 respectively. He holds 12 patents and has authored or co-authored more than 25 publications. From 2003-2006 Daudi worked on process development and yield ramp of IBMs 90nm and 65nm SOI technology nodes. In 2006 he accepted a position in an IBM MSIP design team working on high speed SERDES I/O and delivered designs from 65nm down to 14nm. In addition, he played a key role representing the design team in design-technology-enablement interlocks, where he advocated for design team needs. In April 2015 Daudi left IBM to take a role in Qualcomm's Data Center Group with technical oversight of all SoC development activities related to and dependent on Silicon technology. He provided technical direction to the team through concept, design, tape-out, and new product introduction of the industry's first ARM-based Server Chip in 10nm (Qualcomm Centriq 2400). In his current role at Intel, Daudi leads development of technical strategies and methodologies to achieve increase analog yield and ensure high quality analog validation. He provides technical direction for Server HSIO post-Si validation and is actively involved in developing the next generation of Intel technologists. Daudi lives in Austin, TX with his wife, son (12yrs) and daughter (10yrs). He is originally from Kenya and considers the Austin area his second home.

Jueves 8 de Diciembre de 2022, 16:00 horas. Evento virtual.
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